

Compal Confidential

Model Name : ZIUS1(Lenovo)
ZIUS2(NEC)

File Name : LA-B591P

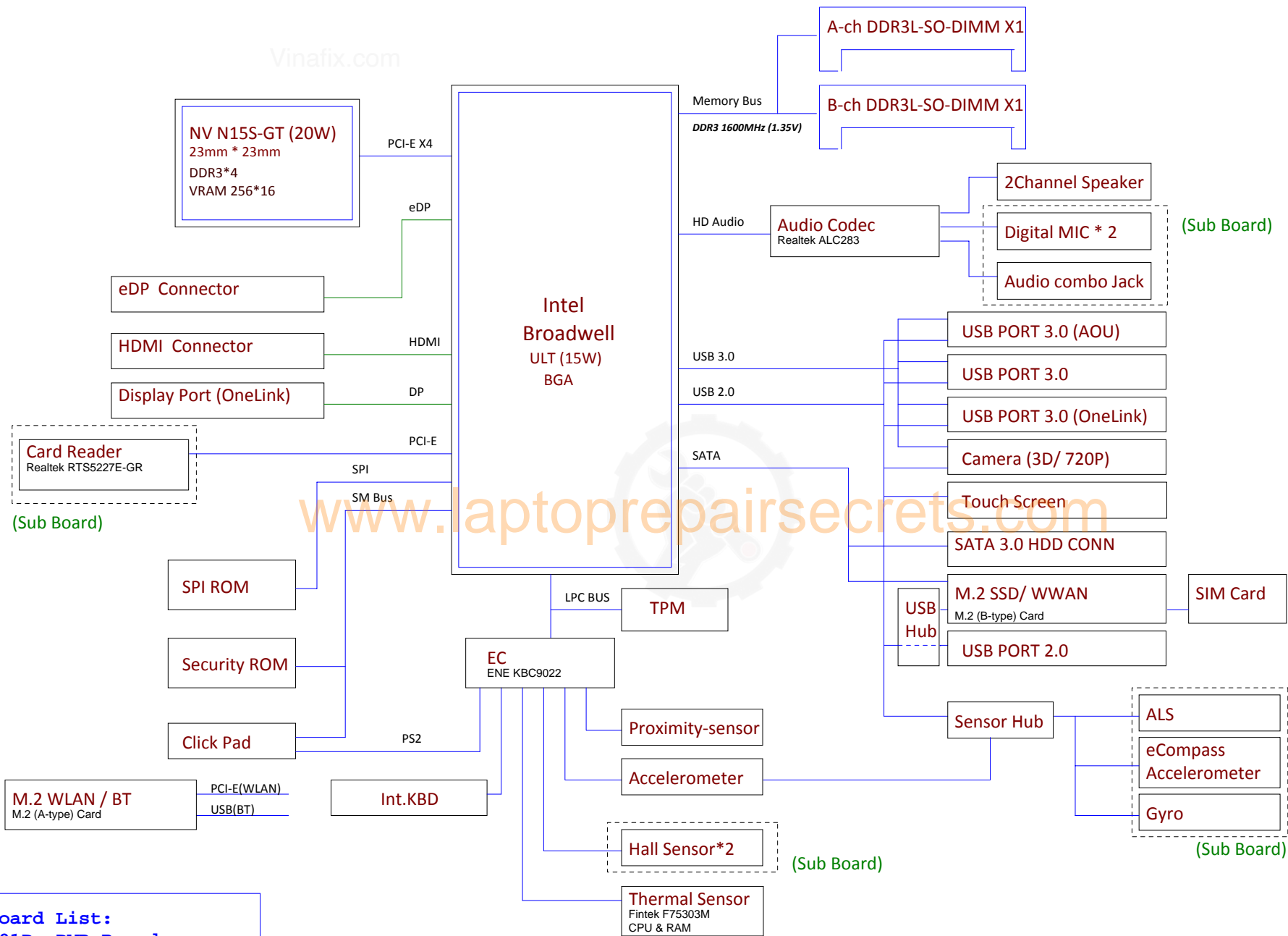
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Asahi M/B Schematics Document

Intel Crescent Bay Broadwell U Processor with DDR3L
+ NVIDIA N15S-GT GPU

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/01/09	Deciphered Date	2014/01/09	Title	Cover Sheet
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				Date	Tuesday, March 25, 2014
				Sheet	1 of 50
				Rev	0.1

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- Sub-Board List:**
- LS-B591P PWR Board
 - LS-B592P Card Reader Board
 - LS-B593P 3D Sensor Board
 - LS-B594P 2D Sensor Board
 - LS-B595P OneLink Board

Voltage Rails

power plane	+B	+5VALW +3VALW	+1.35V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.675VS +1.05VS	+3VM +1.05VM (SBA Only)
S0	○	○	○	○	○ M3 Supported
S3	○	○	○	✗	○ M3 Supported
S5 S4/AC	○	○	✗	✗	○ M3 Supported
S5 S4/ Battery only	✗	✗	✗	✗	
S5 S4/AC & Battery don't exist	✗	✗	✗	✗	

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H
Charger	0001 011X b	12H
Touch HOME button		

EC SM Bus2 address

Device	Address	HEX
Thermal Sensor Fintek F75303M	1001_101xb	9AH
Thermal Sensor ON-semi ADM1032	0100_110xb	4CH
P - Sensor	0010_1000b	28H
Intel BDW-U		
Nvidia N15S-GT		

PCH SM Bus address

Device	Address	HEX
DDR DIMM1	1001 000Xb	A0H
DDR DIMM2		
Security Rom	1010 100xb	A8H
Synaptics Inter Touch Click Pad	0010_110xb	2CH
M.2 mSATA		
M.2 WLAN		

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock	
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON	
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF	
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF	
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF	

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
Unpop	@
Nvidia GPU	DIS@
Intel UMA	UMA@
Micron 2G VRAM	X76M2G@
Hynix 2G VRAM	X76H2G@
Samsung 2G VRAM	X76S2G@
AOAC Mount	AOAC@
w/ 3G	3G@
w/o 3G	NO3G@
Trick Point	TP@
SBA	SBA@
no SBA	NOSBA@
GPU GC6	GC6@
GPU NO GC6	NOGC6@
TPM	TPM@
EMI Un-Mount	@EMI@
EMI Mount	EMI@

CPU

U1	U1	U1
HSW QFSY CPU1@ SA00007AM20	BDW QG21 CPU2@ SA00007Q500	BDW QG22 CPU3@ SA00007OT00

USB 2.0 Port Table

Port	3 External USB Port
0	USB 3.0 AOU Port (MB-Left)
1	USB 3.0 Port (MB-Right)
2	USB 3.0 Port (OneLink)
3	Camera (2D)
4	M.2 BT (w/o 3G) USB2 Hub (w/ 3G)
5	Touch Screen
6	Sensor Hub
7	USB2 Port (MB-Right)

USB 3.0 Port Table

Port	
1	USB 3.0 Port (MB-Left)
2	USB 3.0 Port (MB-Right)
3	USB 3.0 Port (OneLink)
4	Camera (3D)

SATA Port Table

Port	
3	
2	
1	M.2 WWAN/SSD
0	HDD

PCIe Port Table

Port	Lane	
1		
2		
3		M.2 WLAN Card Reader
4		
5	0 1 2 3	GPU
6	0 1 2 3	

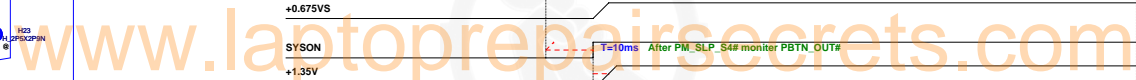
PCB

ZZZ
LA-B591P
DA PCB DA800101000

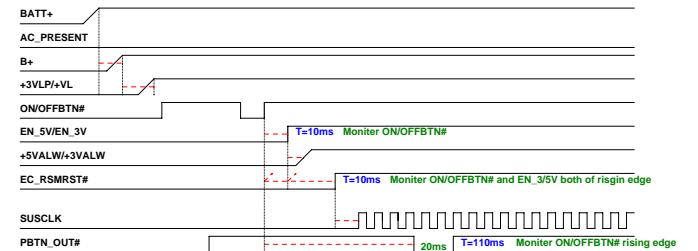
VRAM

ZZZ	ZZZ	ZZZ
Hynix 512MB X76H2G@ X7656639L01	MICRON 512MB X76M2G@ X7656639L02	Samsung 512MB X76S2G@ X7656639L03

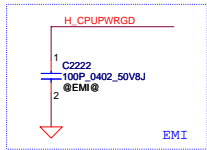
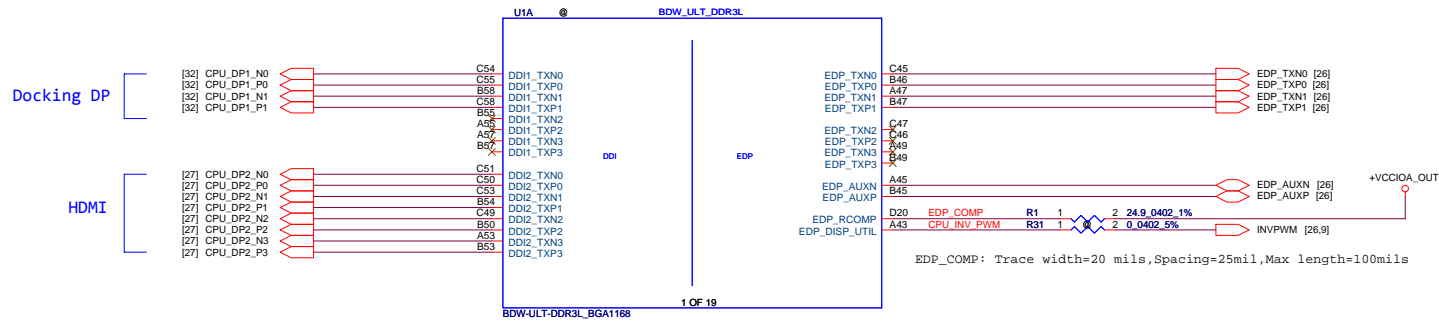
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For R&D				Date: Tuesday, March 25, 2014	Rev 0.1
				Sheet 3 of 50	



[DC Mode]

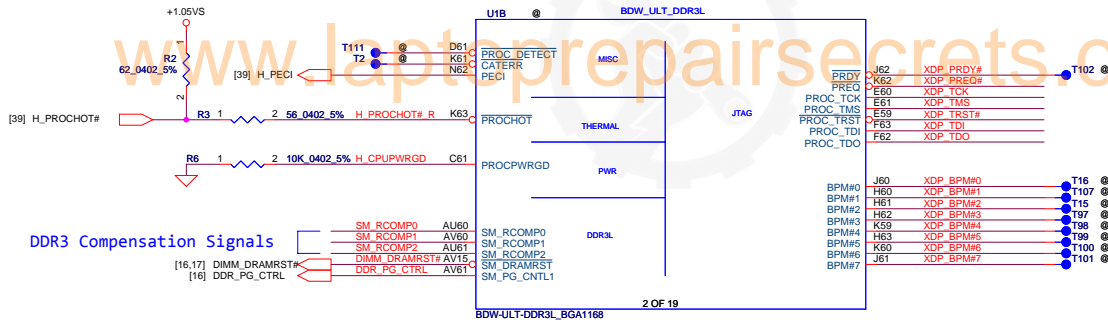
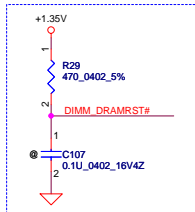
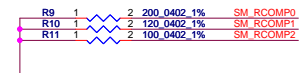


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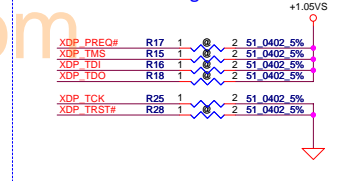


DDR3 Compensation Signals

DDR3 Compensation Signals:
20 mils to comp signals
25 mils to non-comp signals
500 mil for Max trace length



PU/PD for JTAG signals



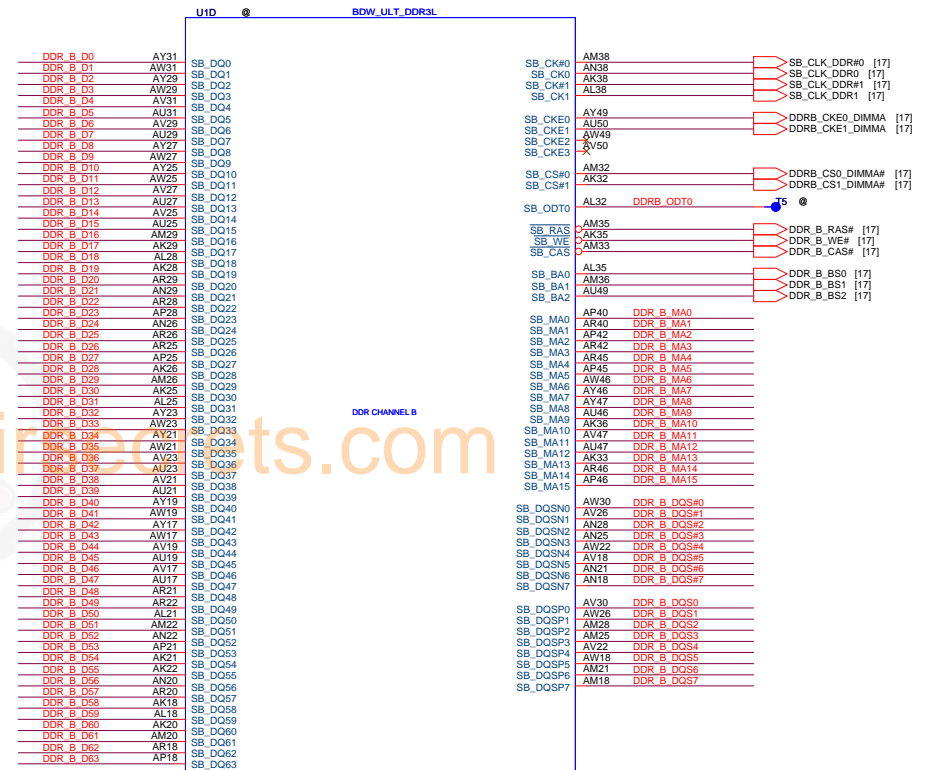
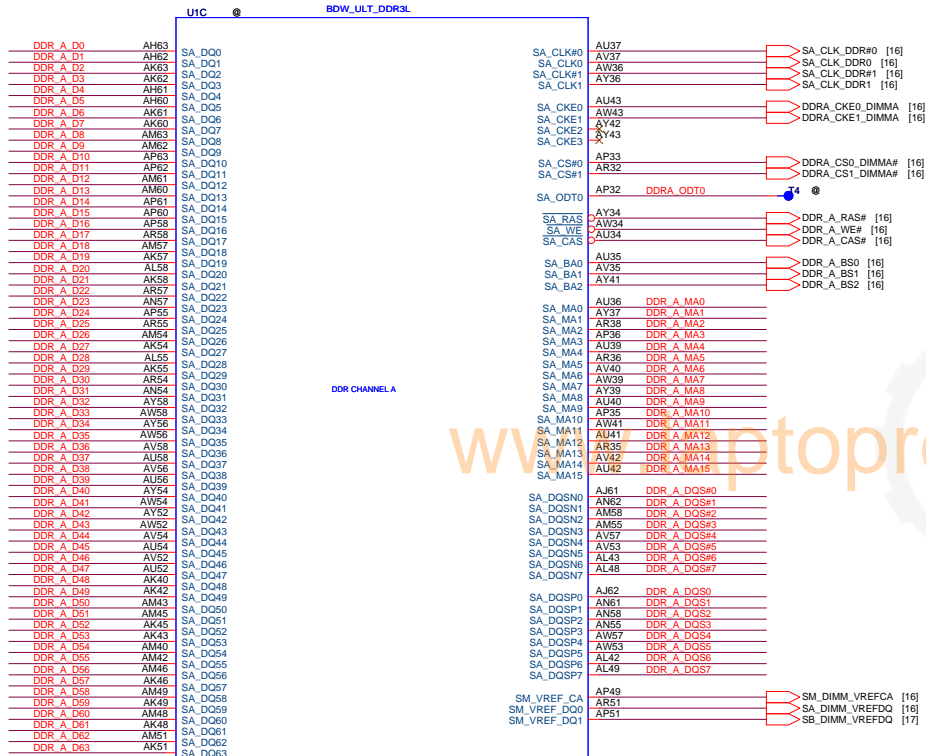
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Date: Tuesday, March 25, 2014				Document Number	LA-B591P SDV
Sheet 5 of 50				Rev	0.1

Memory I/F

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[16] DDR_A_D[0..63]
[16] DDR_A_MA[0..15]
[16] DDR_A_DQS[0..7]
[16] DDR_A_DQS[0..7]

[17] DDR_B_D[0..63]
[17] DDR_B_MA[0..15]
[17] DDR_B_DQS[0..7]
[17] DDR_B_DQS[0..7]



BDW-ULT-DDR3L_BGA1168

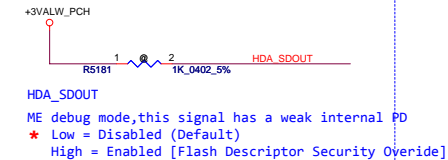
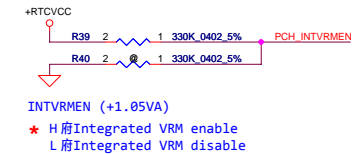
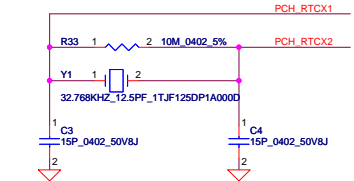
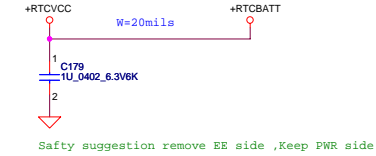
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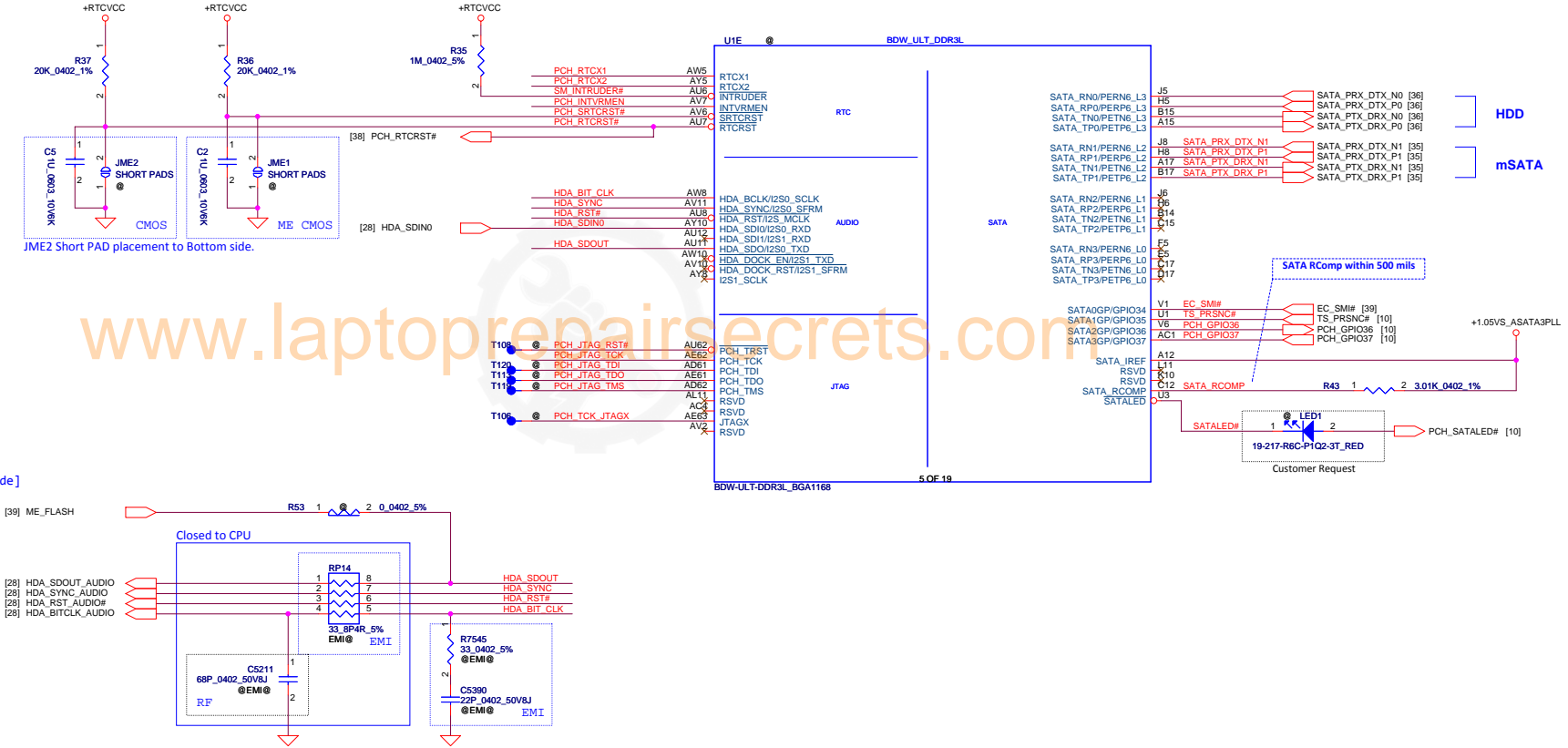
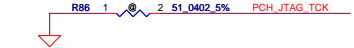
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				Date	Tuesday, March 25, 2014
				Sheet	6 of 50
				Rev	0.1

RTC Battery

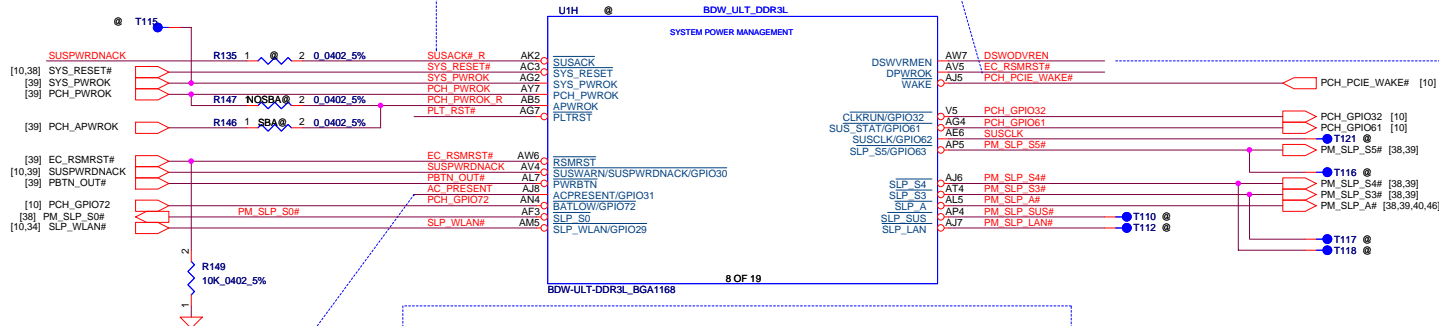


PH/ PD for PCH JTAG



Note: SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit.
CAN be NC ,if not support Deep Sx

DPWROK: Tired togther with RSMRST# that do not support Deep Sx

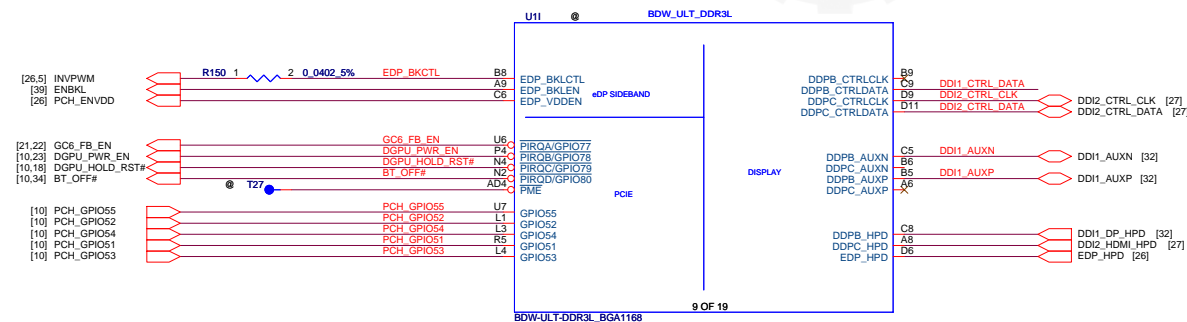
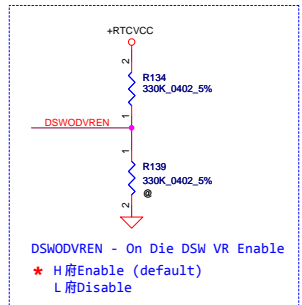
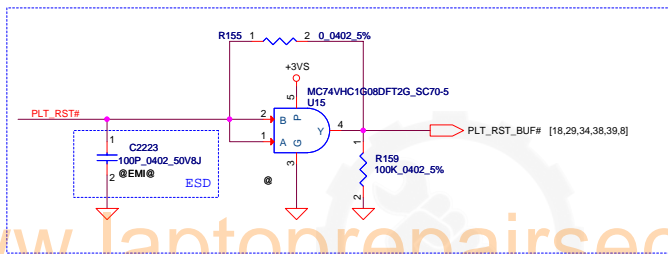


AC_PRESENT Need pull high to VCCDSW3_3
(If no deep Sx, connect to VCCSUS3_3)

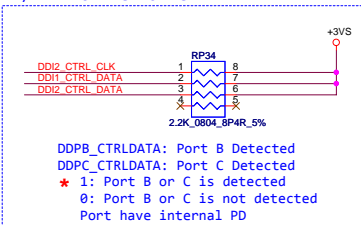
PU 10k @page 10

[10,39] AC_PRESENT

AC_PRESENT

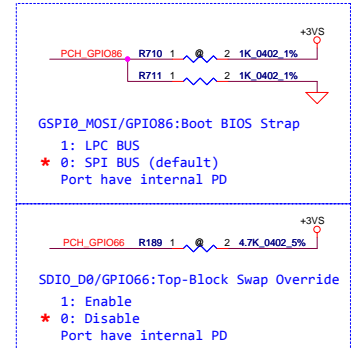
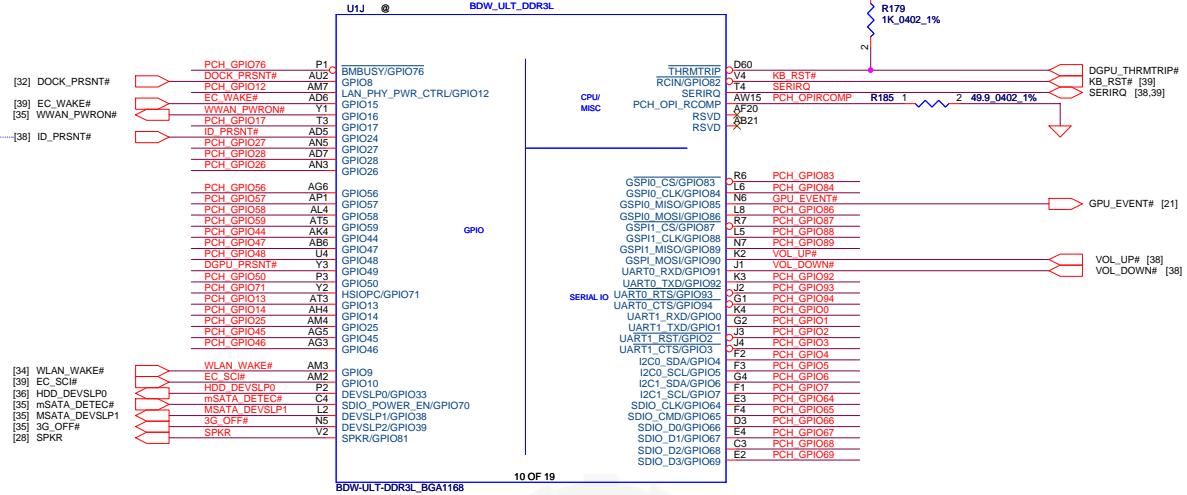
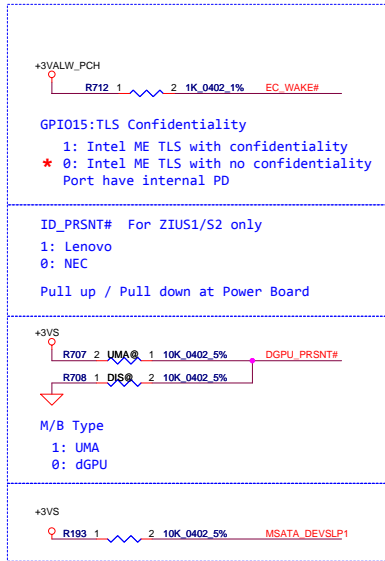


PH/ PD for PCH JTAG

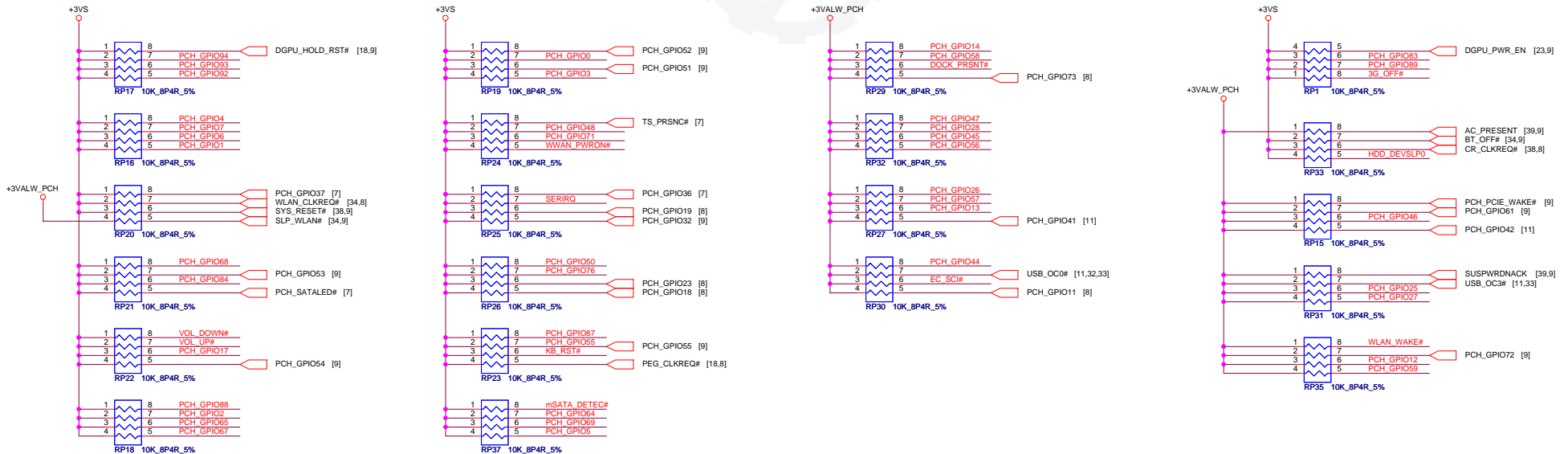


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				Custom	LA-B591P SDV	0.1
				Date:	Tuesday, March 25, 2014	Sheet 9 of 50

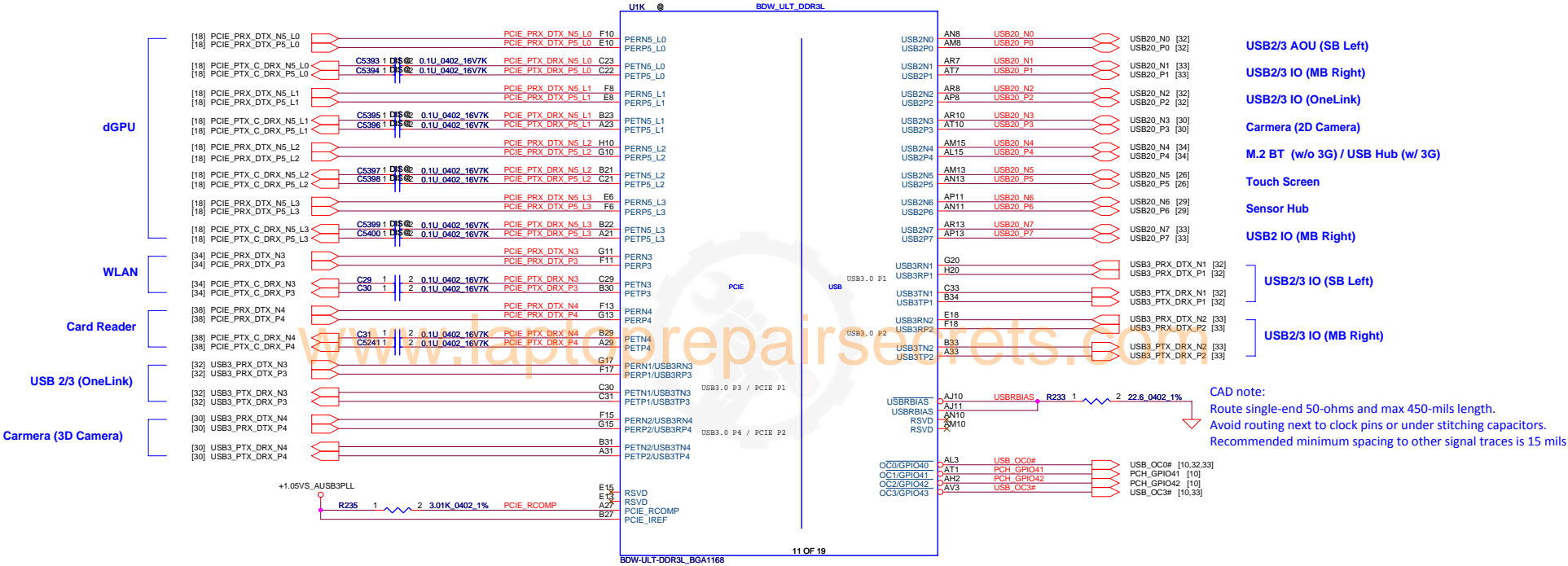
GPIO/ LPIO



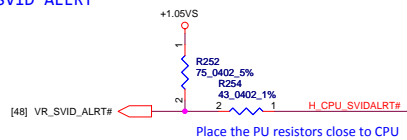
www.laptoprepairsecrets.com



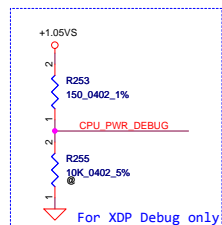
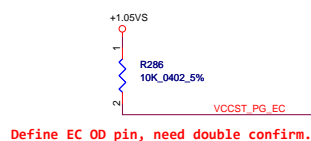
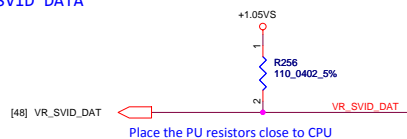
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				Custom	LA-B591P	SDV	0.1
				Date:	Tuesday, March 25, 2014	Sheet	10 of 50



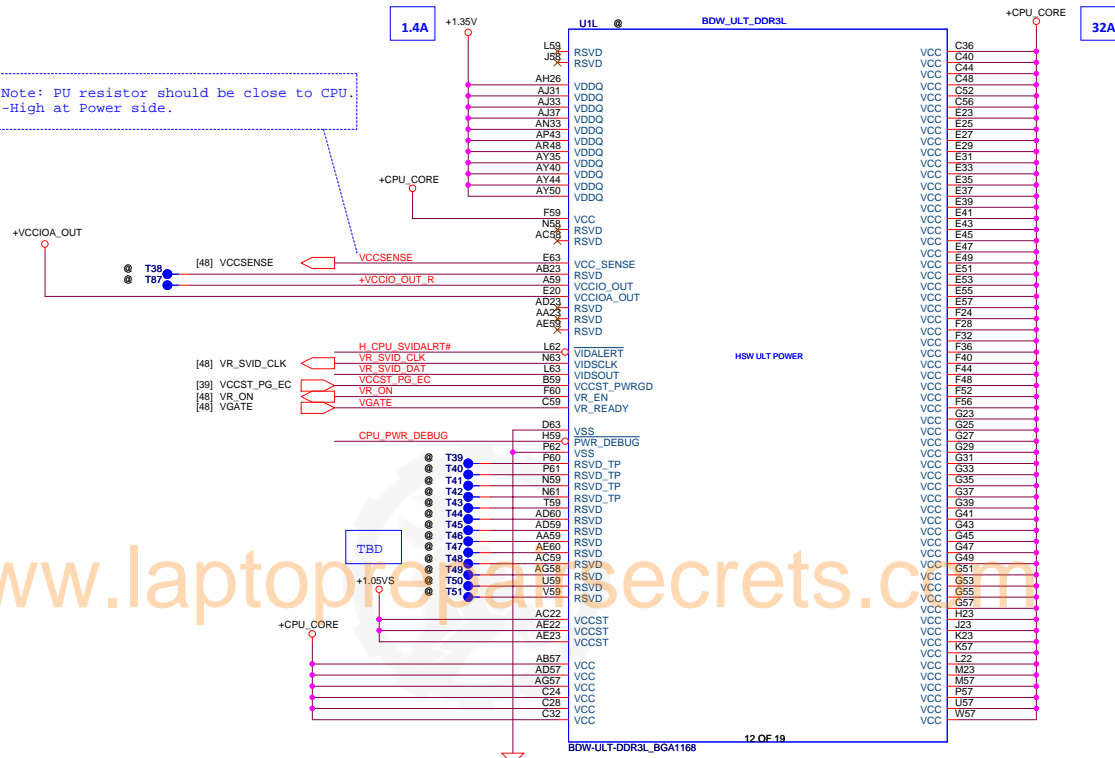
SVID ALERT



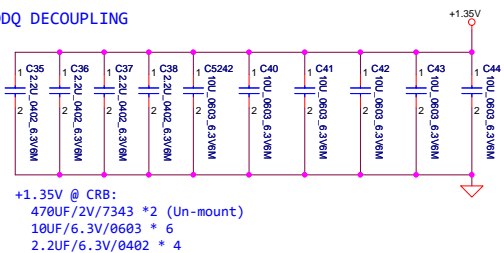
SVID DATA



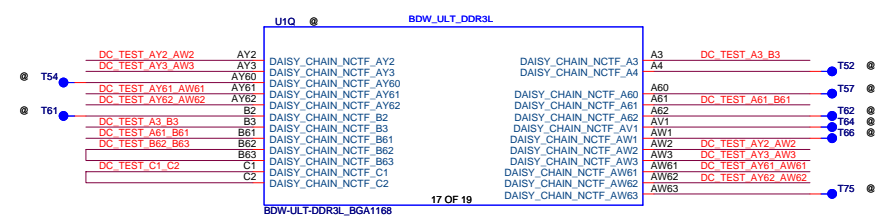
CAD Note: PU resistor should be close to CPU.
Pull-High at Power side.



VDDQ DECOUPLING



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Date: Tuesday, March 25, 2014				Sheet	12 of 50



CFG Straps for Processor

R273 2 1K_0402_1% CFG3

CFG3 - Physical Debug Enable (DFX Privacy)

★ 1: DISABLED

0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR.

CFG3 have internal PU.

R274 2 1K_0402_1% CFG4

CFG4 - Display Port Presence Strap

1 : Disabled; No Physical Display Port attached to Embedded Display Port

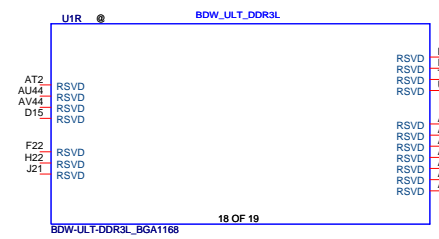
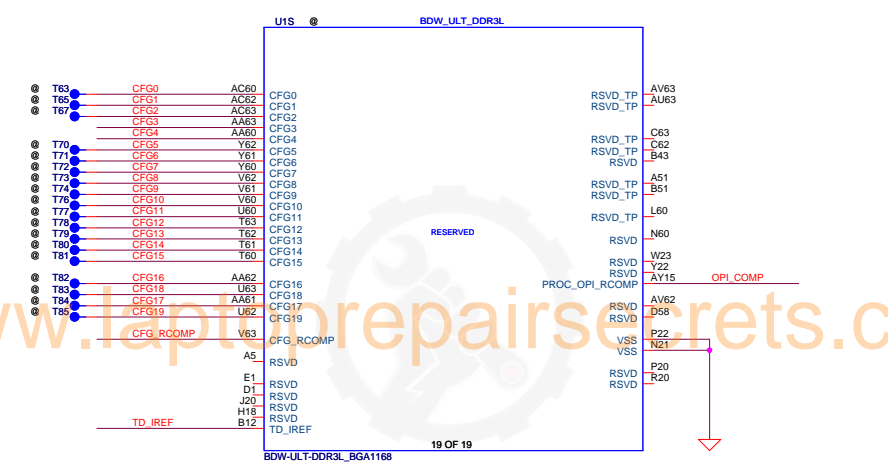
★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

CFG4 have internal PH.

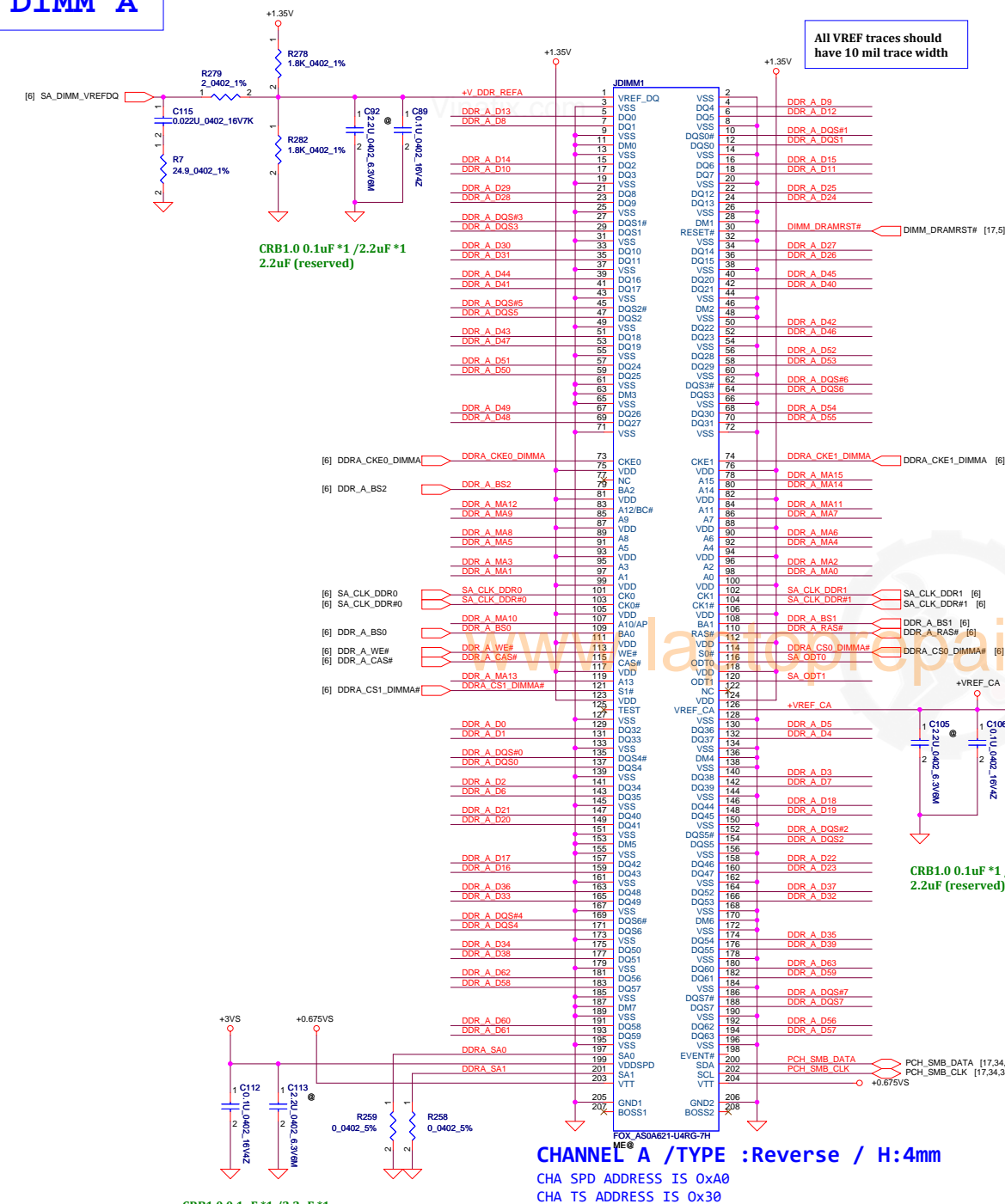
R275 2 49.9_0402_1% CFG_RCOMP

R276 2 49.9_0402_1% OPI_COMP

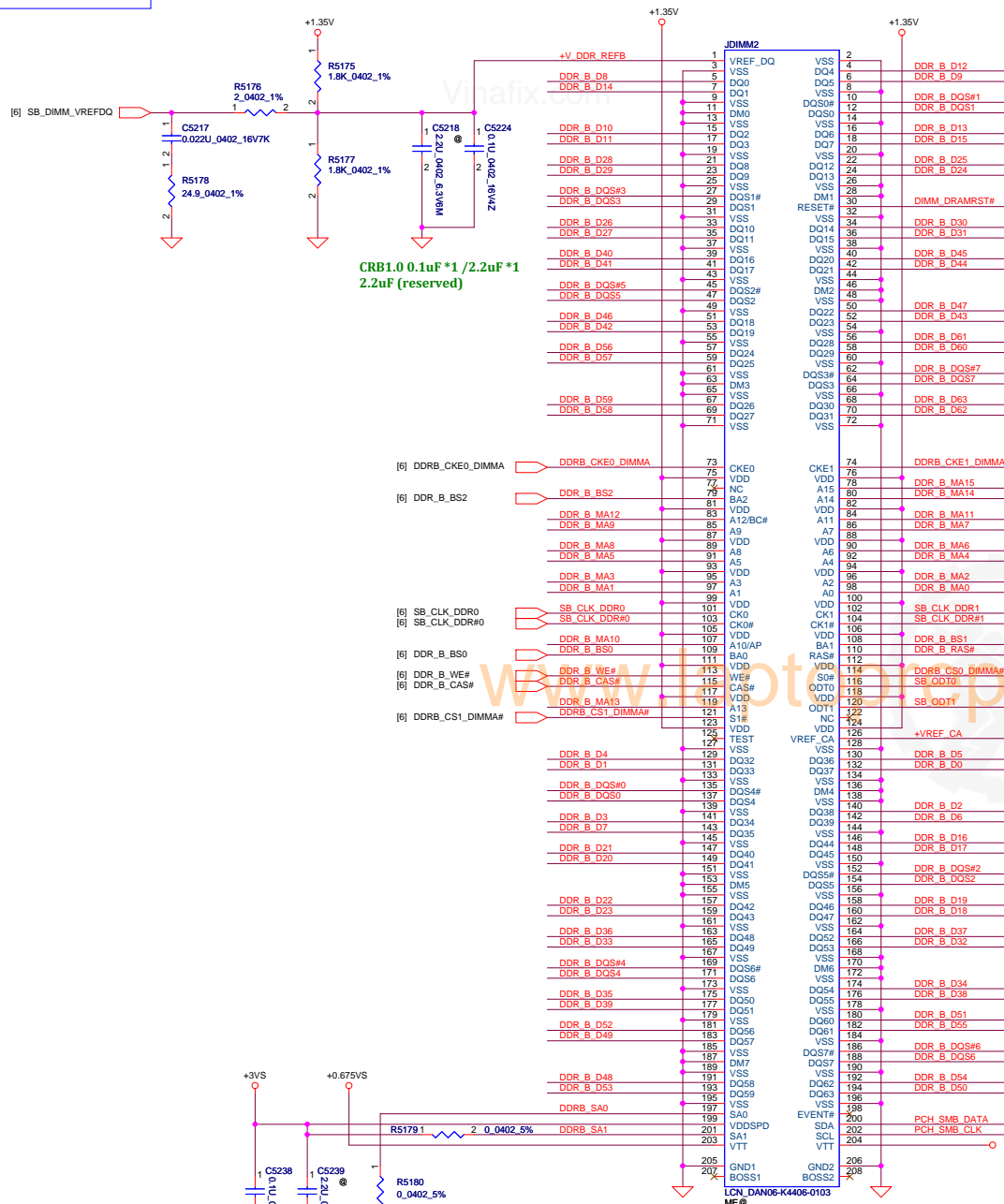
R277 2 8.2K_0402_5% TD_IREF



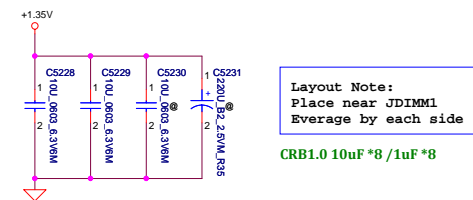
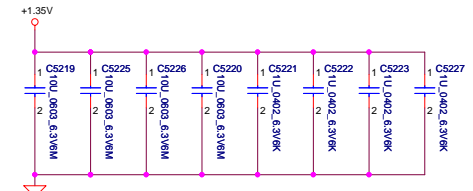
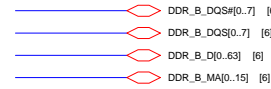
DIMM A



DIMM B

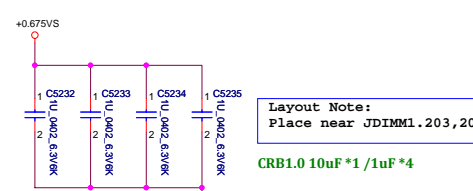


All VREF traces should have 10 mil trace width



Layout Note:
Place near JDIMM1
Everage by each side

CRB1.0 10uF *8 / 1uF *8



Layout Note:
Place near JDIMM1.203,204

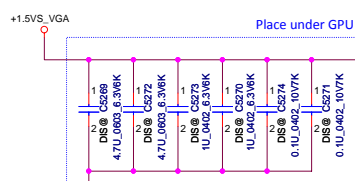
CRB1.0 10uF *1 / 1uF *4

CHANNEL B / TYPE :Reverse / H:4mm

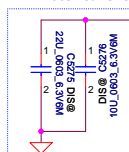
CHB SPD ADDRESS IS 0xA4
CHB TS ADDRESS IS 0x34

P/N:SP07000LT00

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				Sheet	17 of 50



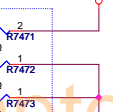
Place near GPU



U200
COMMON
1314 FBVDDQ

FB_CAL_PD_VDDQ D22
FB_CAL_PU_GND C24
FB_CALTERM_GND B25
N155-GT_FCBGA595
DIS@

Place near balls



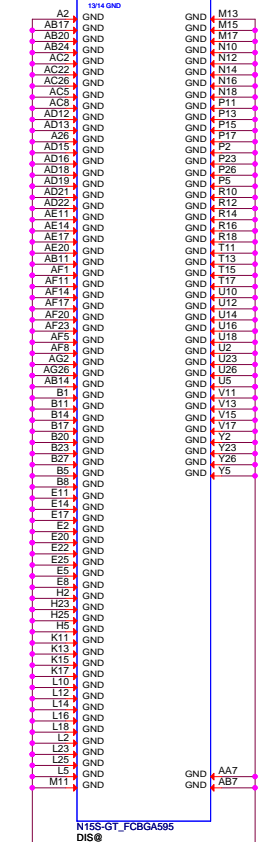
GPU_Decoupling CAPS
@ Power Page

+VGA_CORE
Voltage by GPU SKU

U20E
COMMON
1314 NVDDQ

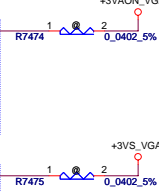
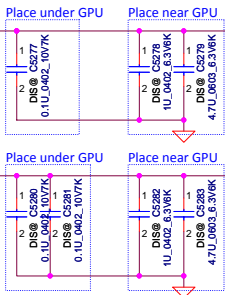
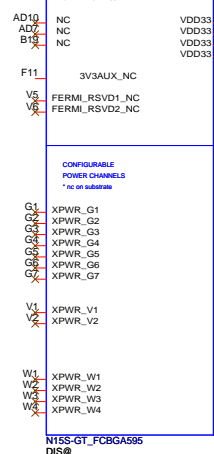
N155-GT_FCBGA595
DIS@

U20F
COMMON
1314 GND



N155-GT_FCBGA595
DIS@

U20C
COMMON
1414 XVDVDDQ3

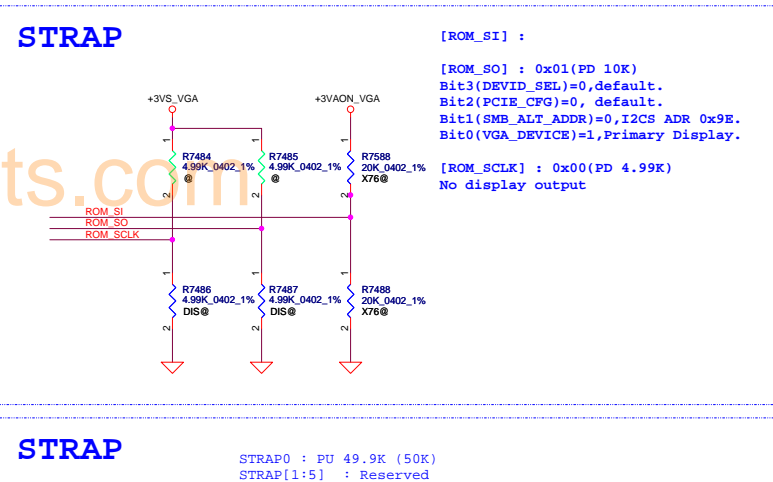
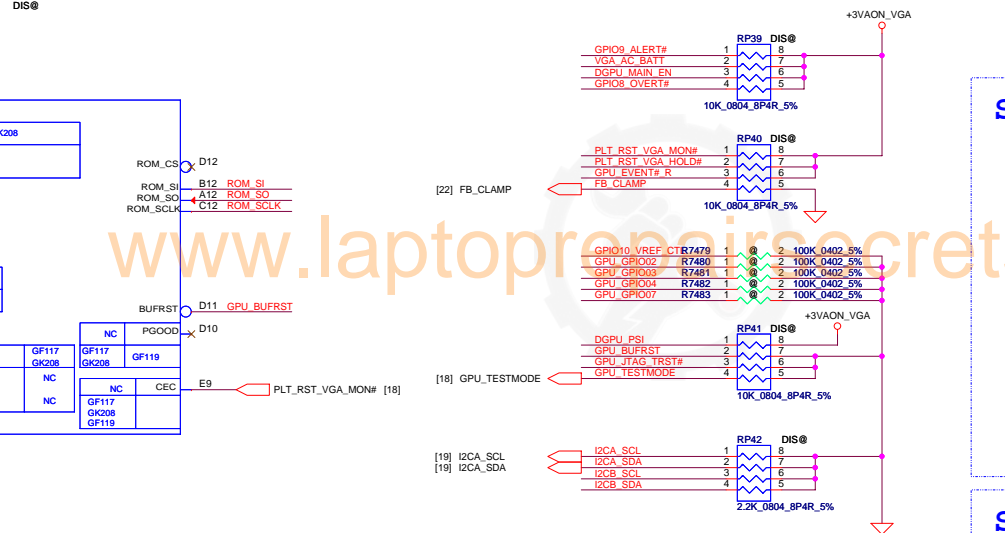


** XPWR pins are configurable.
These pins are not connected on the substrate.
Therefore, XPWR pins can be assigned as needed,
to improve Top layer routing, power delivery.

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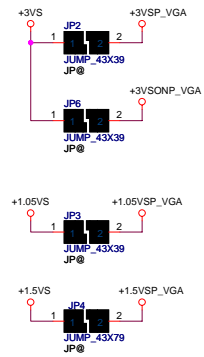
For BSC using,

T2108	TP0	GPU_JTAG TCK	AE5	JTAG_TCK
T2109	TP0	GPU_JTAG TMS	AD6	JTAG_TMS
T2110	TP0	GPU_JTAG TDI	AE6	JTAG_TDI
T2111	TP0	GPU_JTAG TDO	AF6	JTAG_TDO
T2112	TP0	GPU_JTAG TRST#	AG4	JTAG_TRST

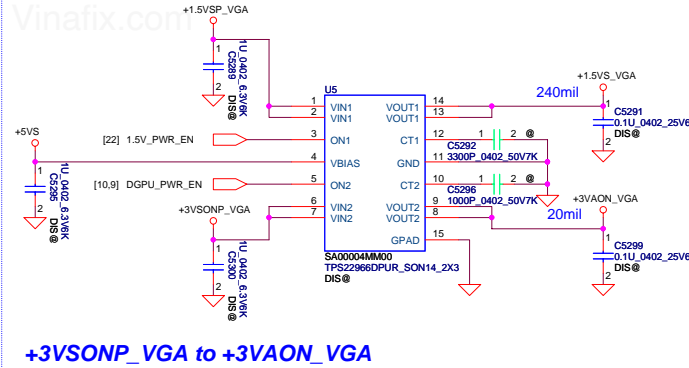


GPU	FB Memory DDR3(1.5V) / DDR3L(1.35V)					ROM_SI	
						R7488 PD	R7588 PU
N15S-GT/GM	128M x16	Hynix	1.5V	1GHz	H5TC2G63FFR-11C	4.99K	NA
		Micron	1.5V	1GHz	MT41J128M16JT-093G:K DateCode_Min:1332	10K	NA
		Samsung	1.5V	1GHz	K4W2G1646Q-BC1A	15K	NA
	256M x16	Hynix	1.5V	1GHz	H5TC4G63AFR-11C	35K	NA
		Micron	1.5V	1GHz	MT41J256M16HA-093G:K DateCode_Min:1332	45K	NA
		Samsung	1.5V	1GHz	K4W4G1646D-HC1A	NA	4.99K

For Power consumption Measurement

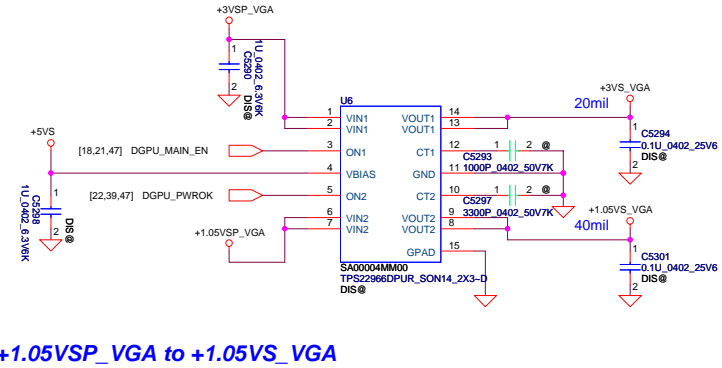


+1.5VSP_VGA to +1.5VS_VGA

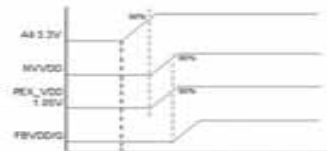


+3VSONP_VGA to +3VAON_VGA

+3VSP_VGA to +3VS_VGA



+1.05VSP_VGA to +1.05VS_VGA



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are asserted

Figure 3-6. Example of Power-up Sequencing Order

Note:

- The ramp time for any rail must be more than 40 μs, and is recommended to be less than 2ms.

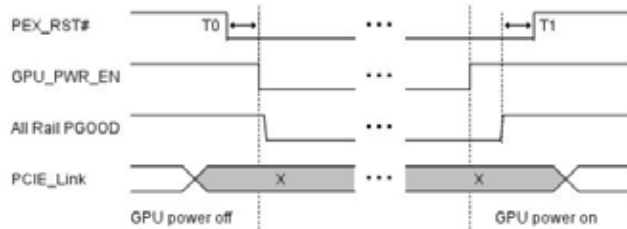


Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

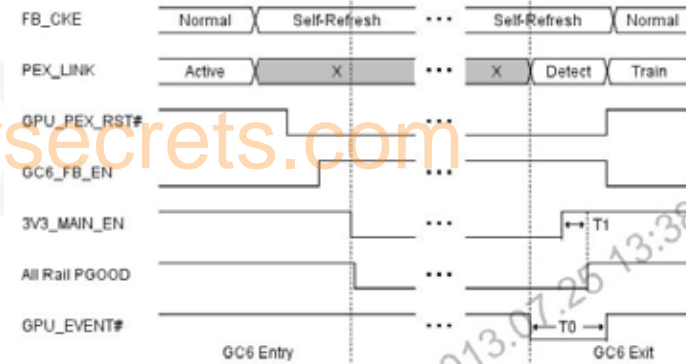


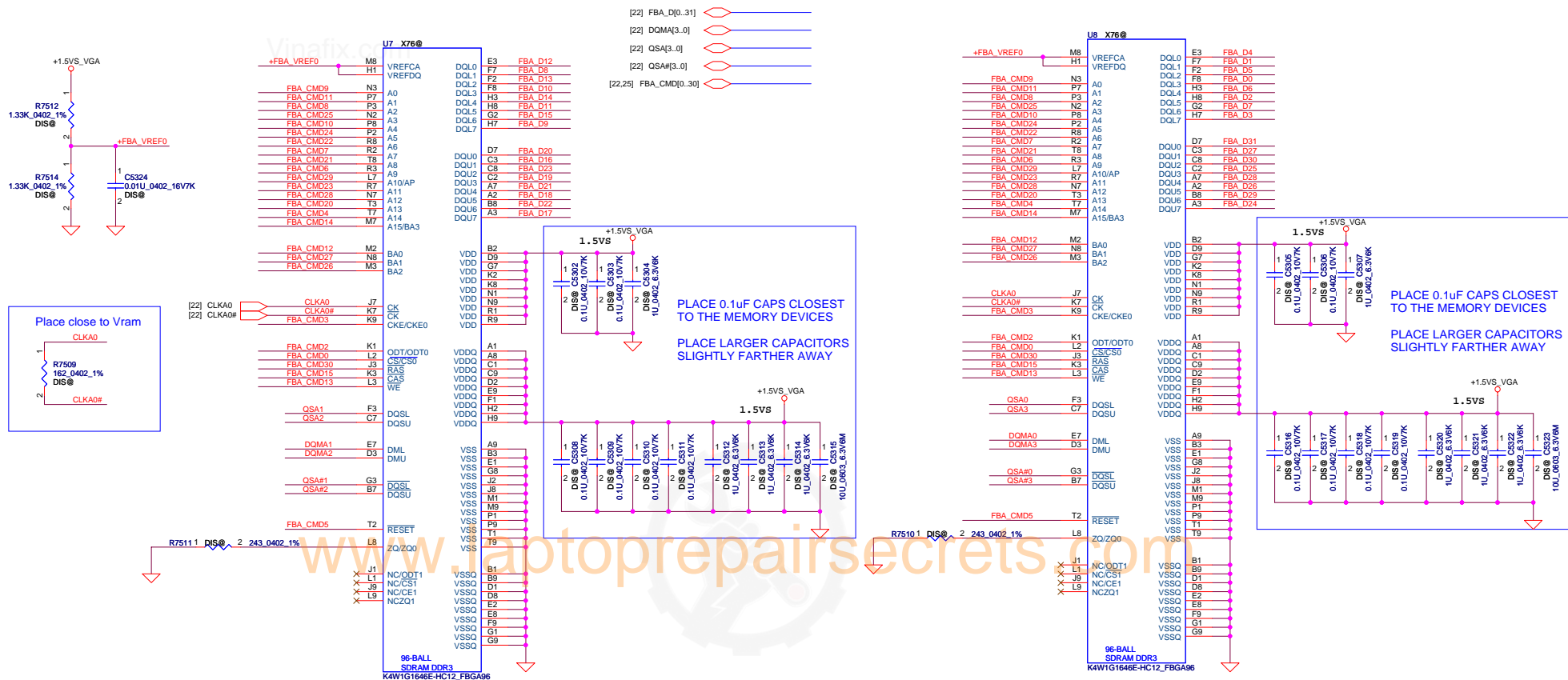
Figure 18-15. GC6 2.0 Entry/Exit Sequence Timing Diagram

Table 18-3. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	11/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

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Memory Partition A - Lower 32 bits [31..0]



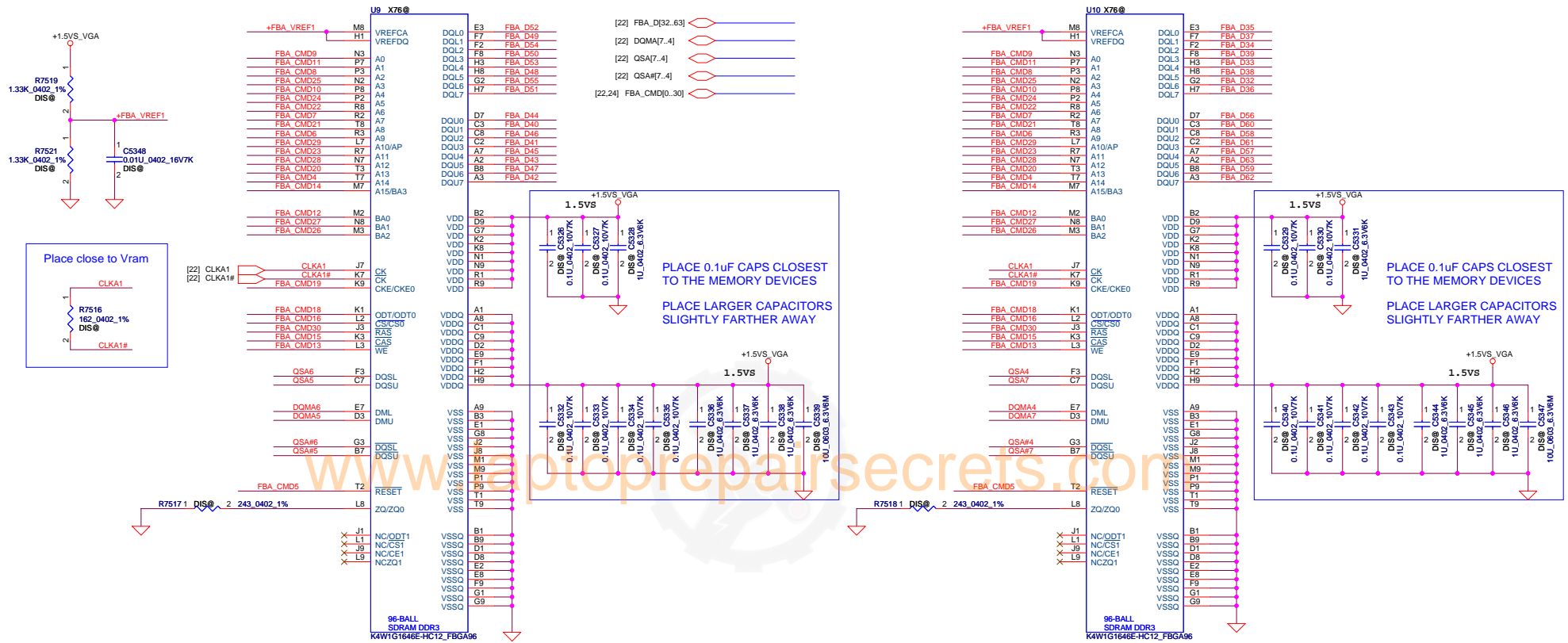
A15 is not required for any x16 device, even up to 4Gb density.

A15 is only needed if we support x8 configurations, and only at 4Gb.

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Memory Partition A - Upper 32 bits [64..32]

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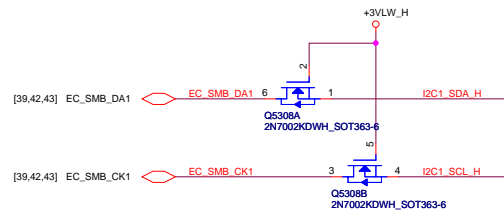
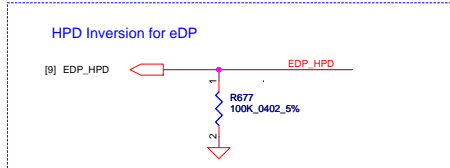
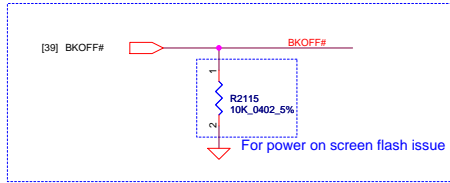


A15 is not required for any x16 device, even up to 4Gb density.
A15 is only needed if we support x8 configurations, and only at 4Gb.

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eDP Panel Conn

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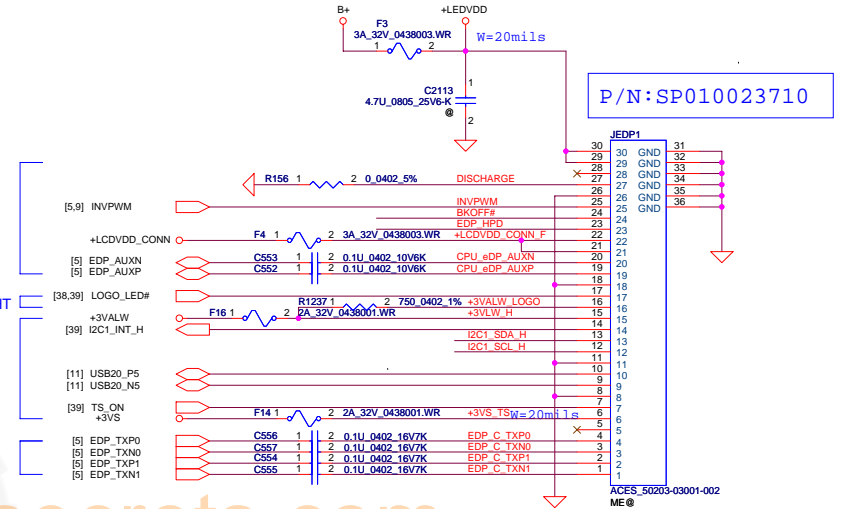


LCD Panel

A LOGO RED LIGHT

Touch Panel Vibrator

LCD Panel

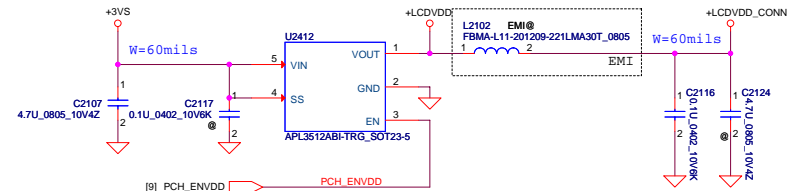


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LCD POWER CIRCUIT

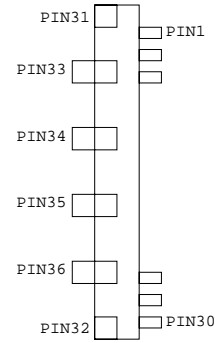
SS table

Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS



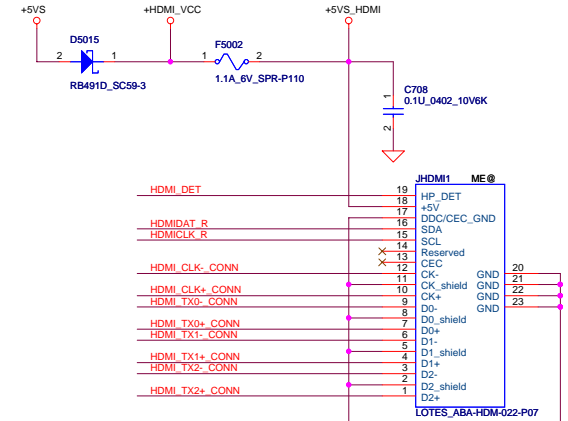
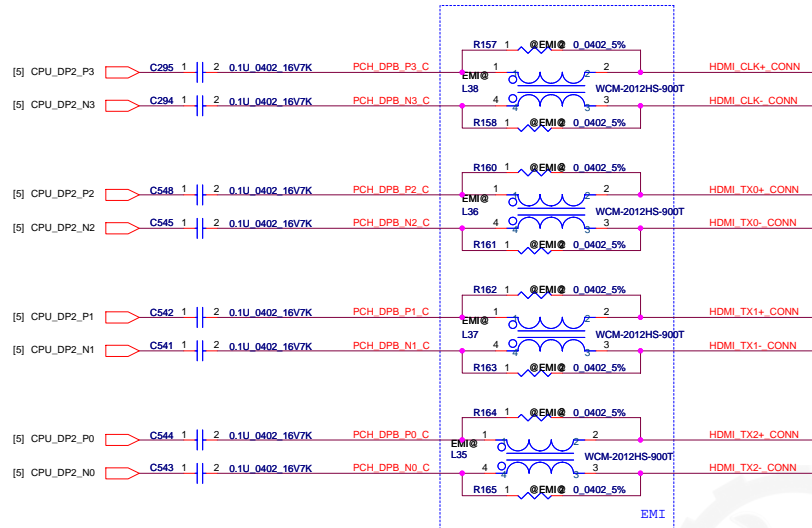
Touch Panel & Vibrator module pin define

No	Pin define
1	VCC (5V)
2	D+
3	D-
4	+3VS
5	GND
6	+3VALW
7	I2C1_SCL_H
8	I2C1_SDA_H
9	I2C1_INT_H
10	GND

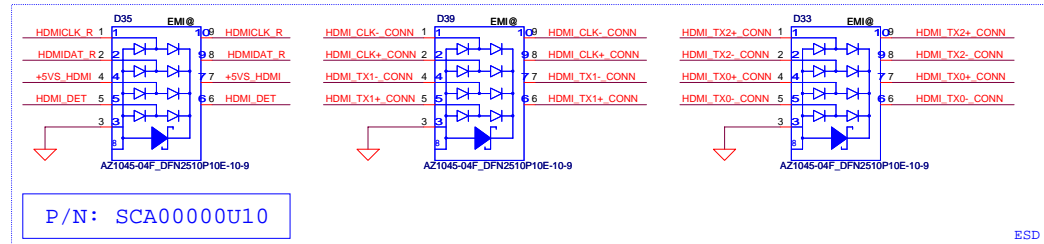
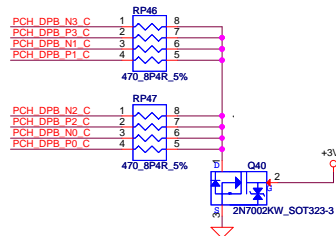
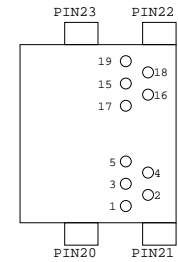
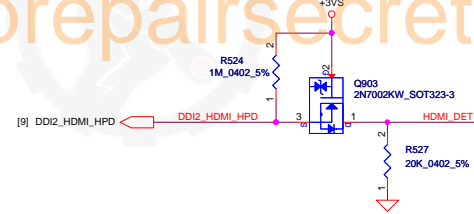
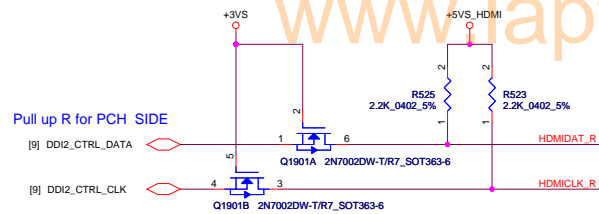


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P/N: SM070003Y00



P/N: DC232000B10
TYPE A Connector

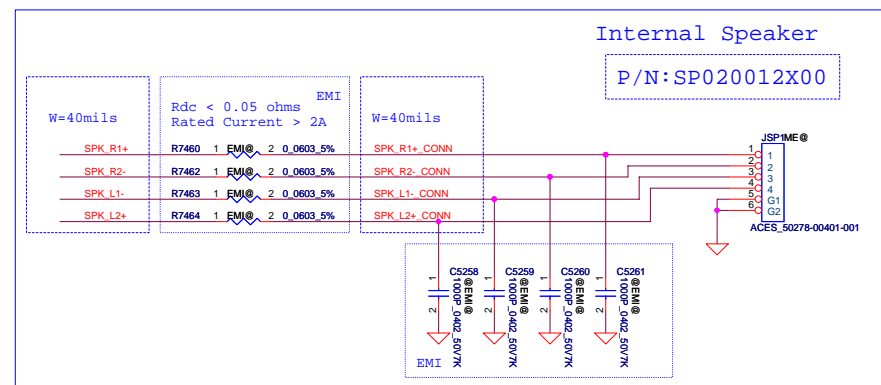
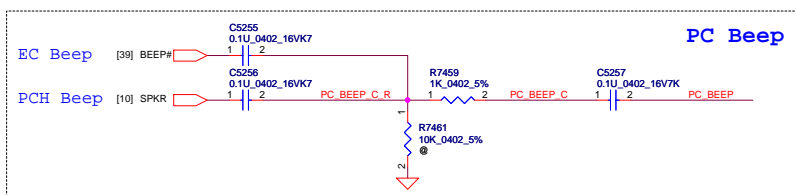
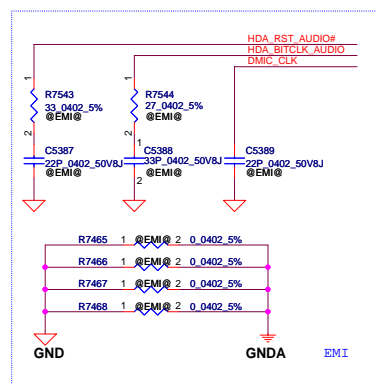
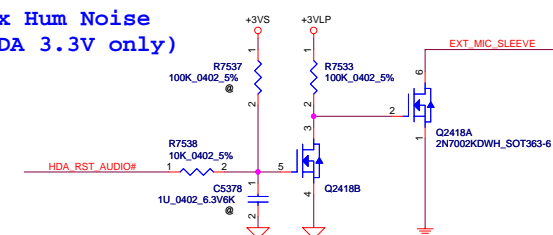
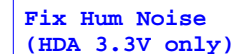
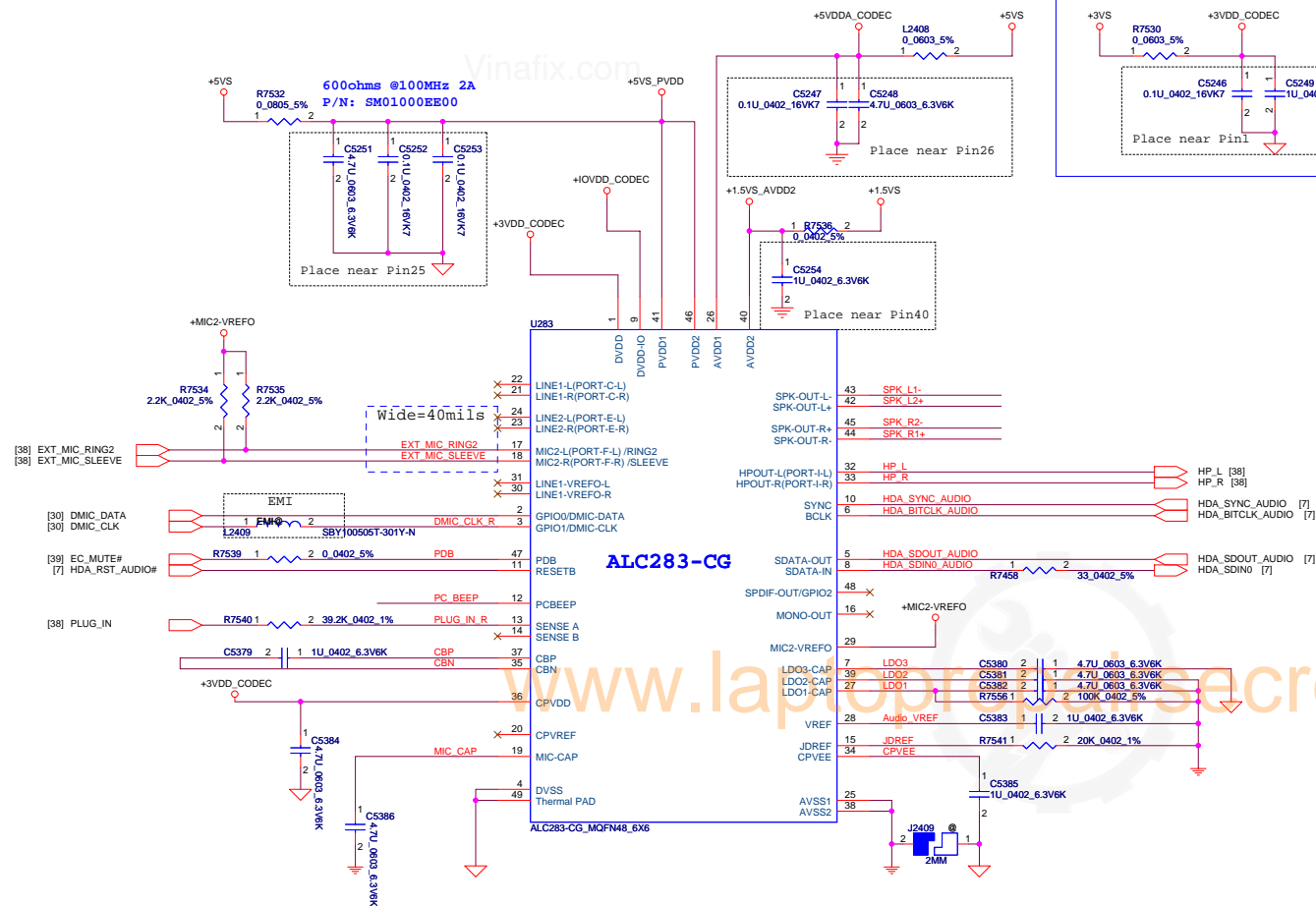


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ESD

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Date:	Tuesday, March 25, 2014	Sheet	27	of	50

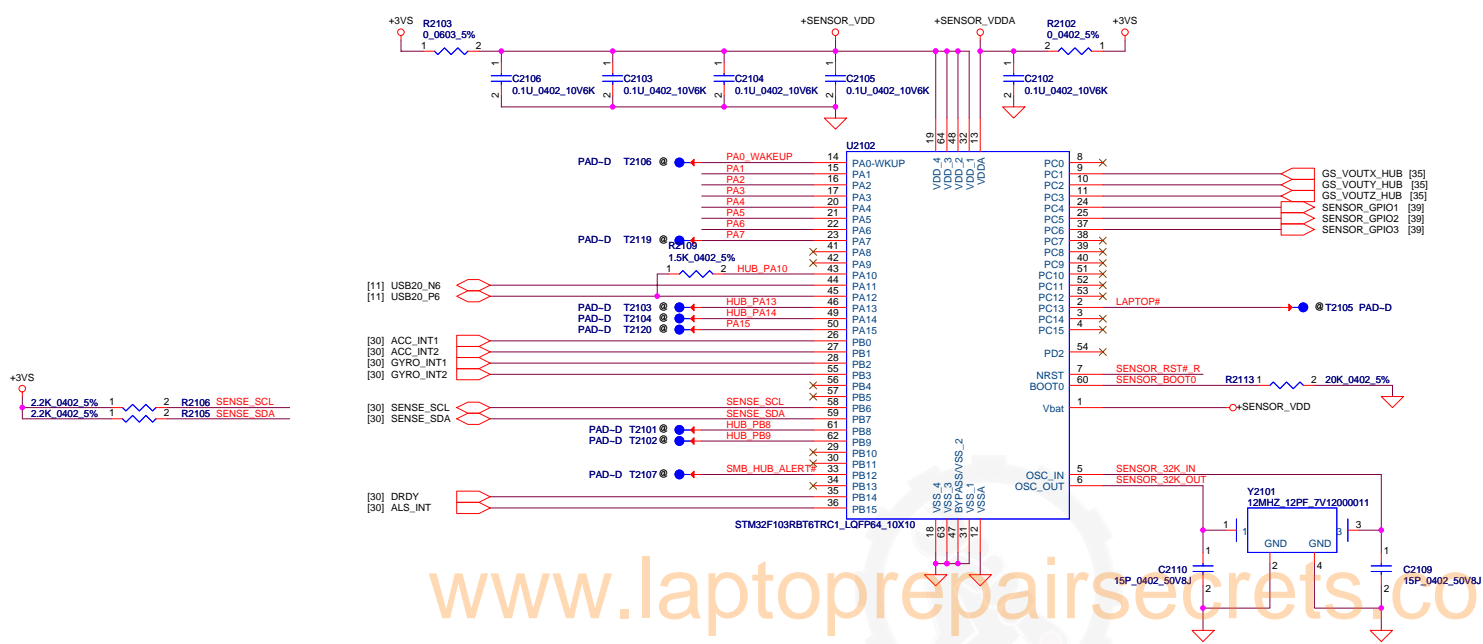
Audio ALC283



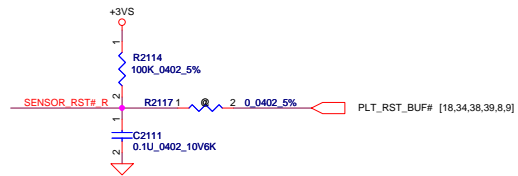
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Sensor Hub

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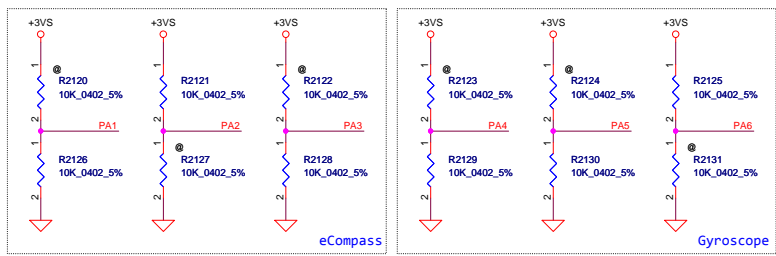


Mode	SENSOR_GPIO1 (EC_GPIO13)	SENSOR_GPIO2 (EC_GPIO4C)	SENSOR_GPIO3 (EC_GPIO15)
Notebook	0	0	0
Flat	0	0	1
Stand	0	1	0
Tent	0	1	1
Tablet	1	0	0



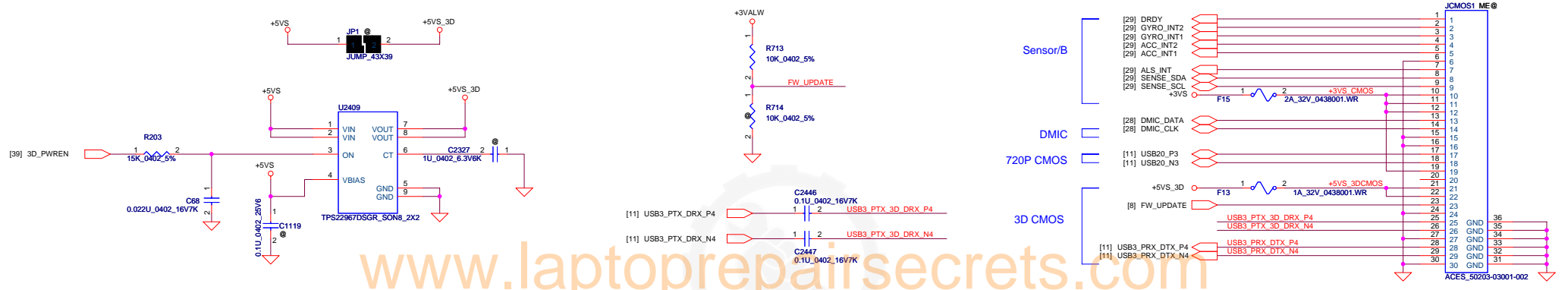
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GPIO	Orientation Definition
PA1	303_l (eCompass)
PA2	303_m
PA3	303_n
PA4	4200_l (gyroscope)
PA5	4200_m
PA6	4200_n



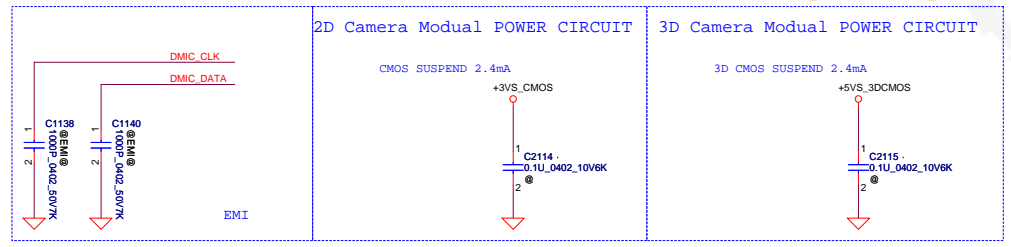
CMOS + Sensor Board Conn

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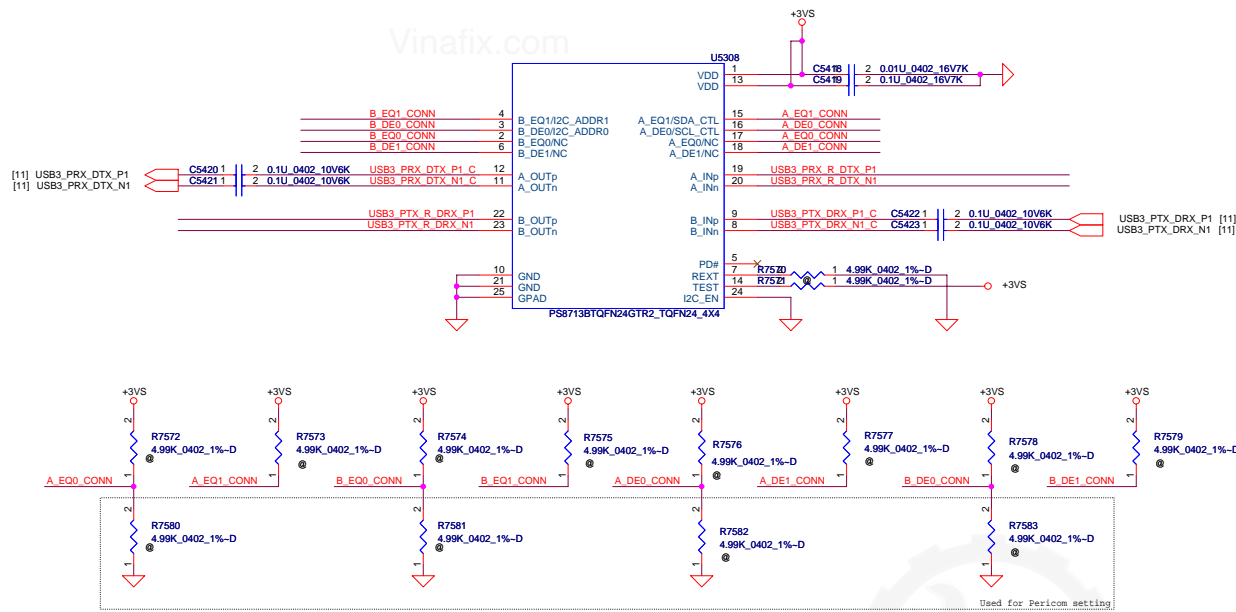
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P/N:SP010023710



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Date	Tuesday, March 25, 2014	Sheet	30	of	50

USB3.0 Redriver (Left)



PERICOM PI3EQX7502AIZDEX SA00006WV00

Equalization	EQ_A / EQ_B
3 dB	Low
6dB (Default)	Open
9dB	High

De-Emphasis	DE_A / DE_B
0 dB	Low
-3.5 dB	Open
-6 dB	High

Parade PS8713BTQFN24GTR2-A1 SA00005OR20

Equalizer	A_EQ1 / B_EQ1 (Internal pull Low)	A_EQ0 / B_EQ0 (Internal pull Low)
9.5 dB	Low	Low
13 dB	Low	High
4.5 dB	High	Low
7.5 dB	High	High

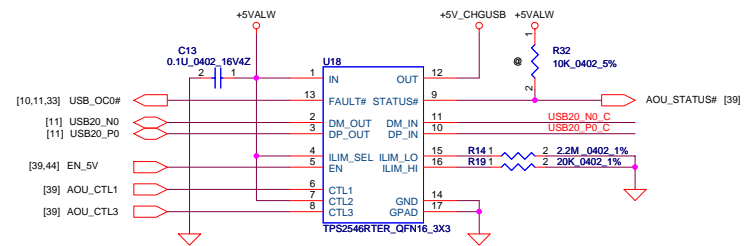
De-Emphasis	A_DE1 / B_DE1 (Internal pull Low)	A_DE0 / B_DE0 (Internal pull Low)
3.5dB	Low	Low
No	Low	High
2.7dB	High	Low
5dB	High	High

TEST (Internal pull Low)	
Normal operation (default)	Low
Test mode enable	High

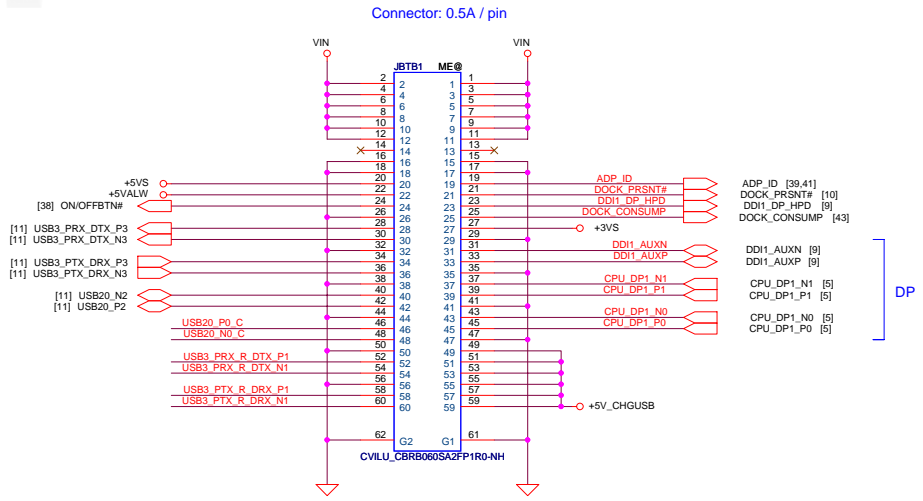
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Docking Board BtB Conn

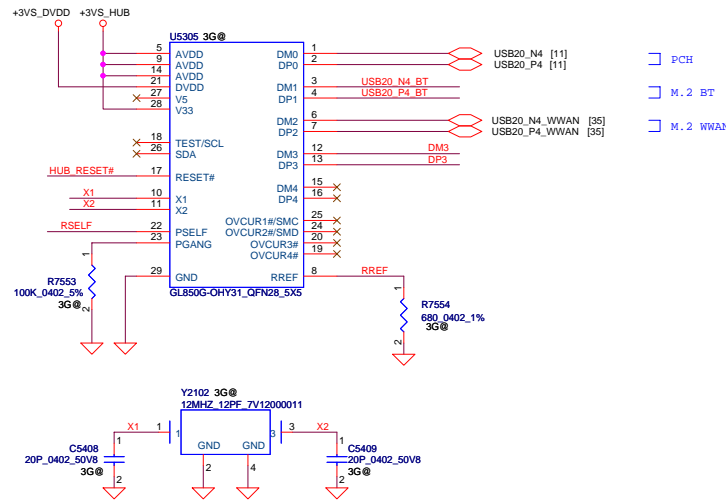
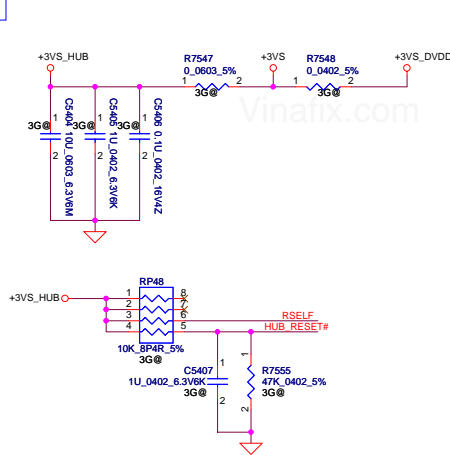
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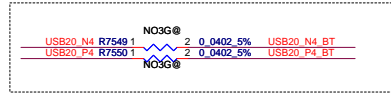
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- USB2.0 to Docking
- USB2.0 to Connector
- USB3.0 to Connector



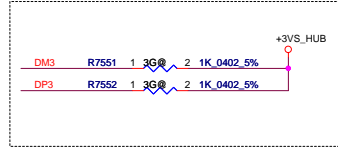
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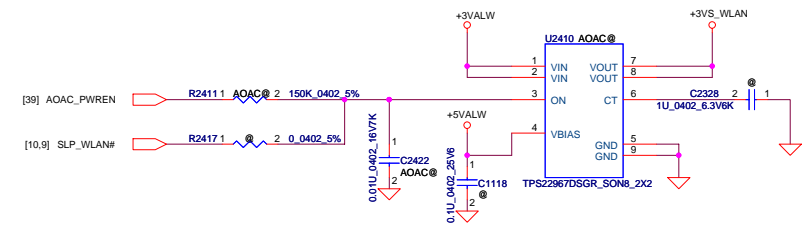
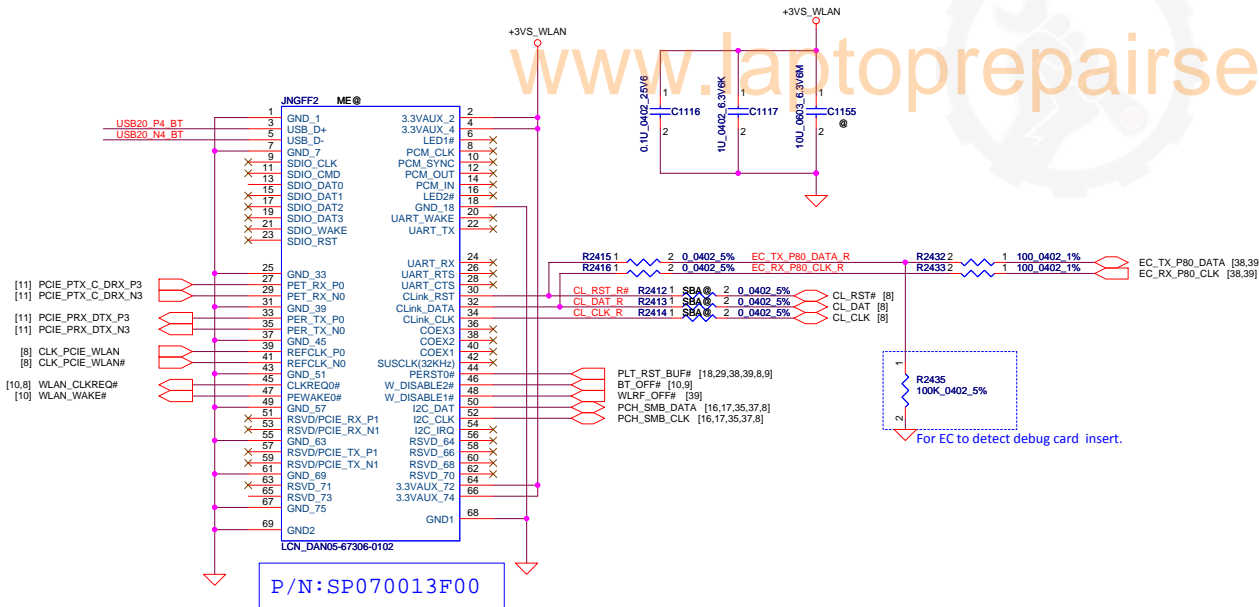
Bypass Resistance



Disable Port 3 & Port 4



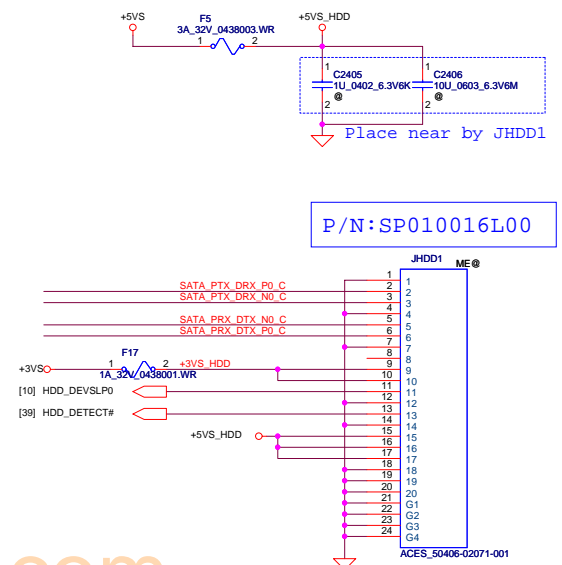
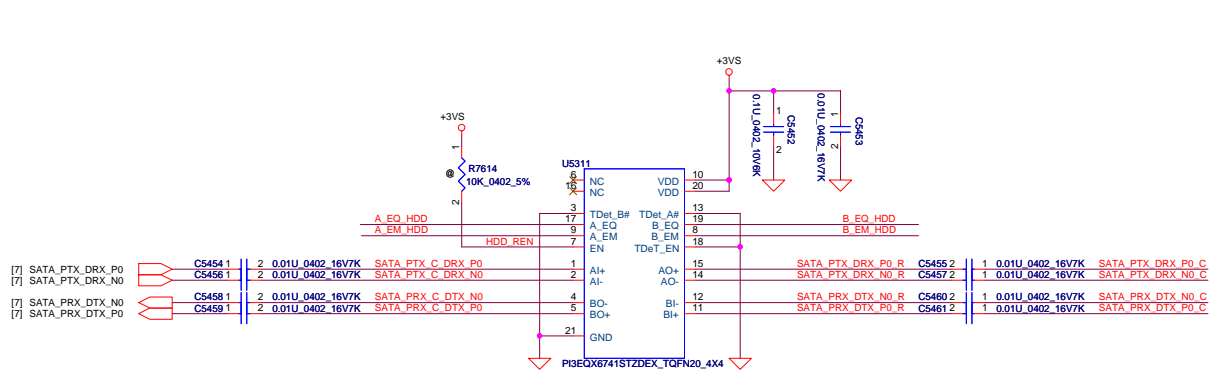
M.2 WLAN



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				Sheet	34 of 50

SATA HDD WTB Conn

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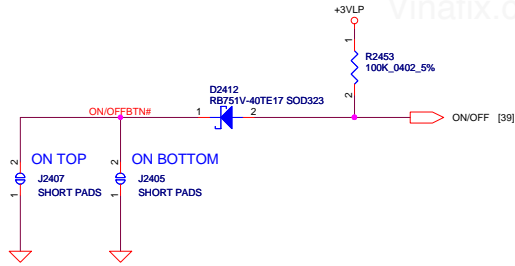
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PERICOM PI3EQX6741STZDEX
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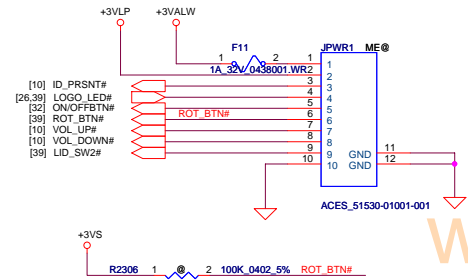
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6dB (Default)	Open
9dB	High

Output Pre-Emphasis	A_EM / B_EM
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1.5 dB	High

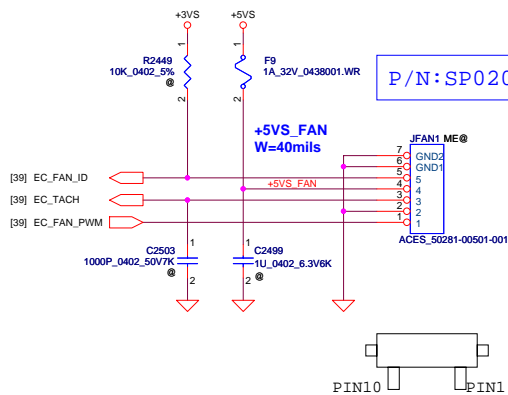
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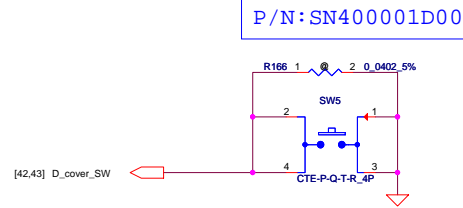


FAN Conn



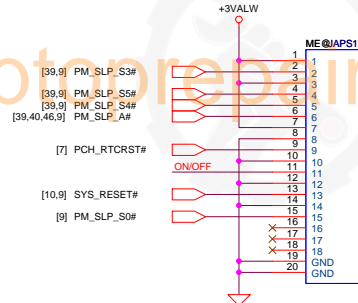
P/N: SP020014V00

D_Cover cut Power

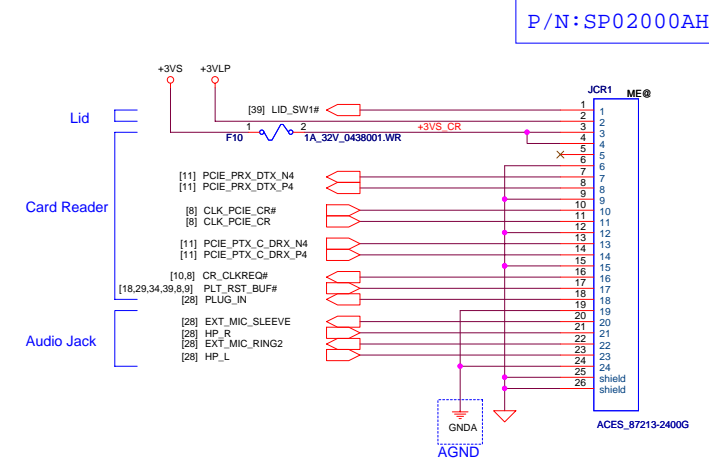


P/N: SN400001D00

Debug Conn

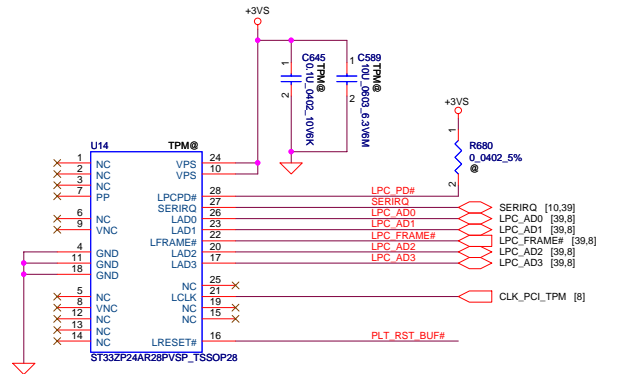


Card Reader Conn



P/N: SP02000AH00

TPM



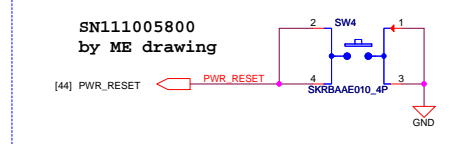
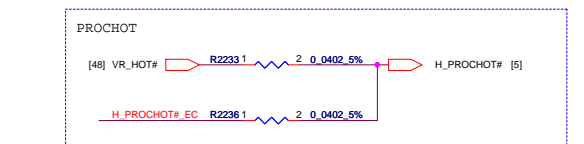
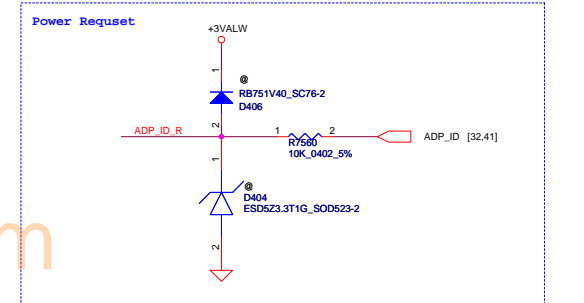
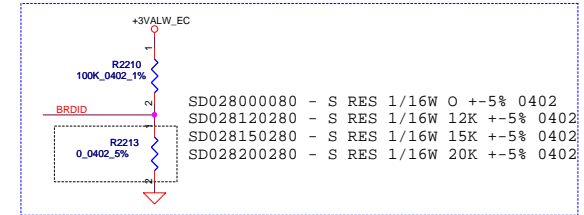
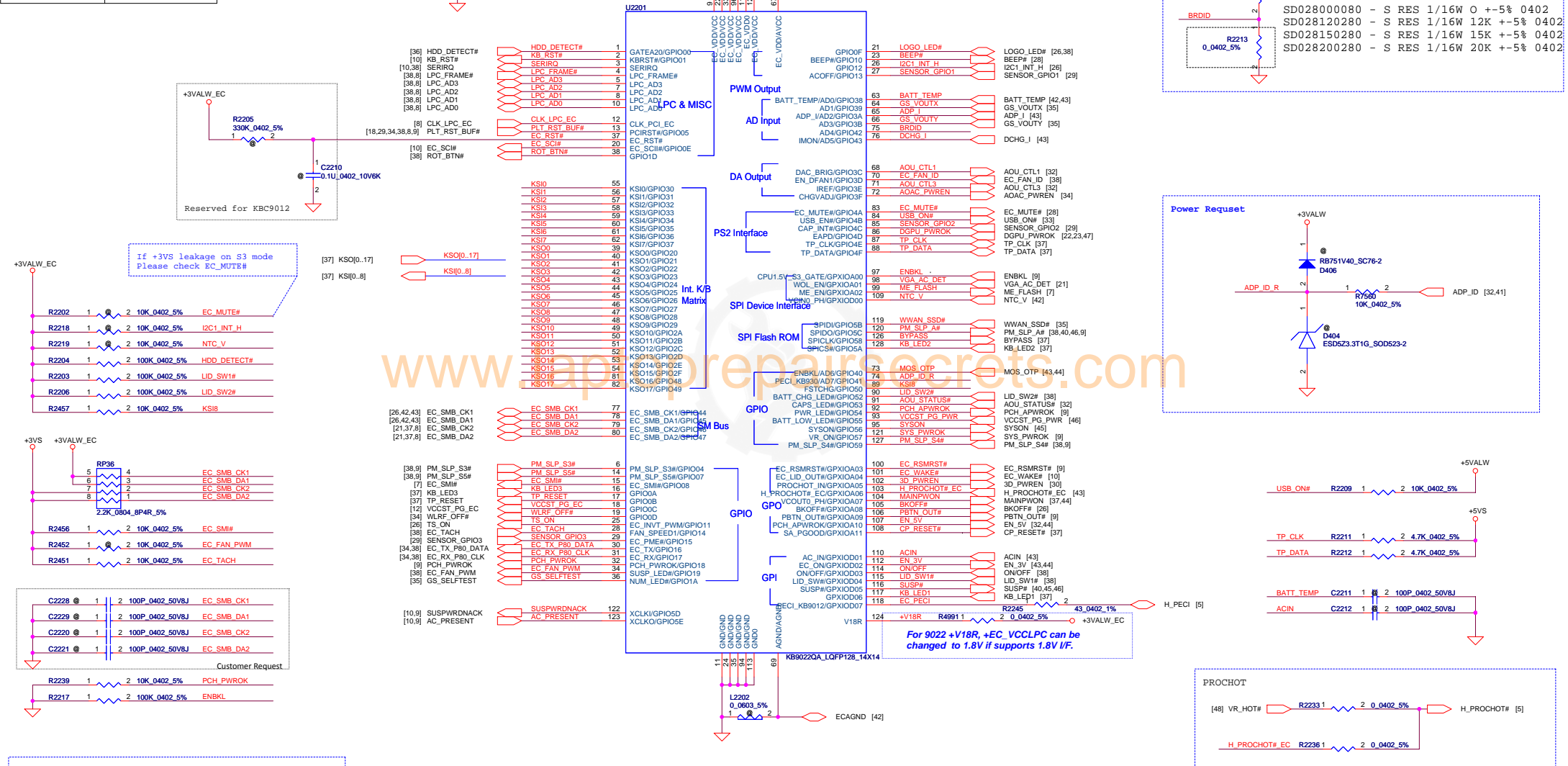
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/01/09	Deciphered Date	2014/01/09	Title	PBTN/FAN/TPM/RTC/IO Board
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				Document Number	LA-B591P SDV
				Date	Tuesday, March 25, 2014
				Sheet	38 of 50

EC KB9022

KB9022 A v.02

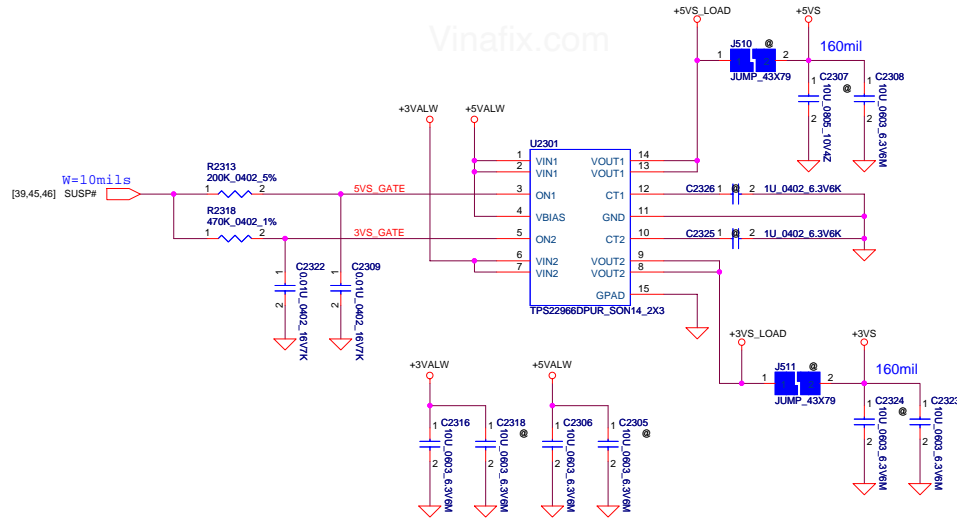
GPIO W/O internal-PH:

1. GPIO44	6. GPIO4B
2. GPIO45	7. GPIO4E
3. GPIO46	8. GPIO4F
4. GPIO47	9. GPIO50
5. GPIO4A	10. GPIO51



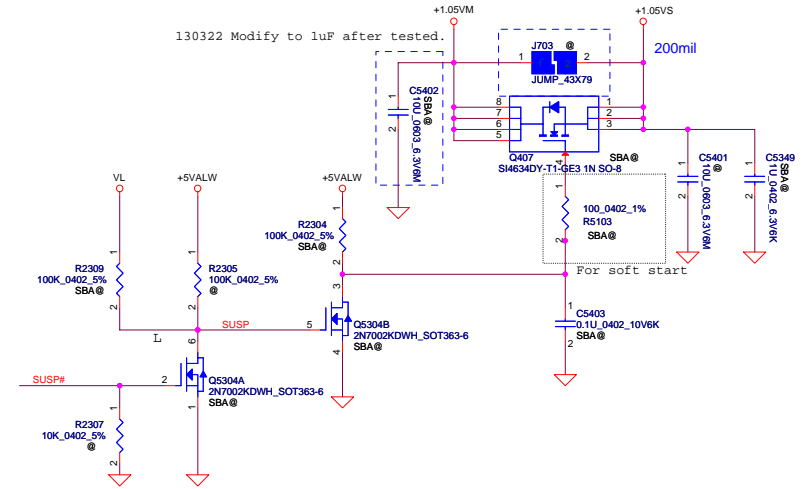
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Issued Date	2014/01/09	Deciphered Date	2014/01/09	Title	EC ENE-KB9022
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Date		Tuesday, March 25, 2014		Sheet	39 of 50

+5VALW TO +5VS
+3VALW TO +3VS

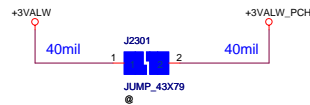


PJ703 Short => NOSBA
PJ703 Open => SBA

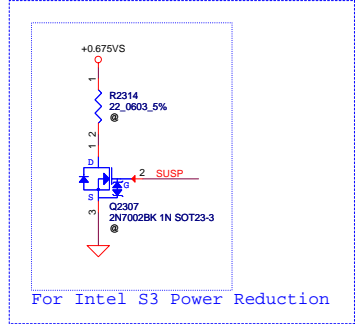
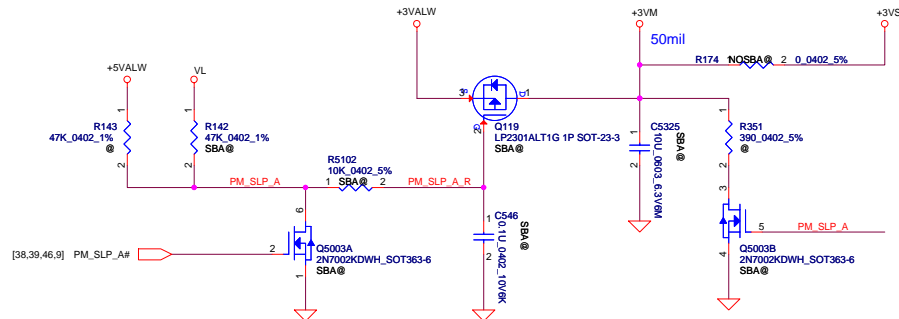
Rds(on) VGS=4.5V, ID=8.5A, 7mOhm (Max)



+3VALW TO +3VALW(PCH AUX Power)



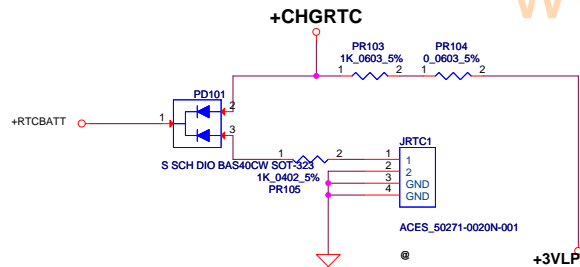
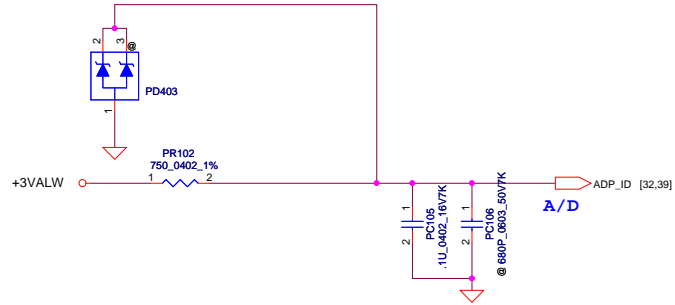
+3VALW TO +3VM (SBA)



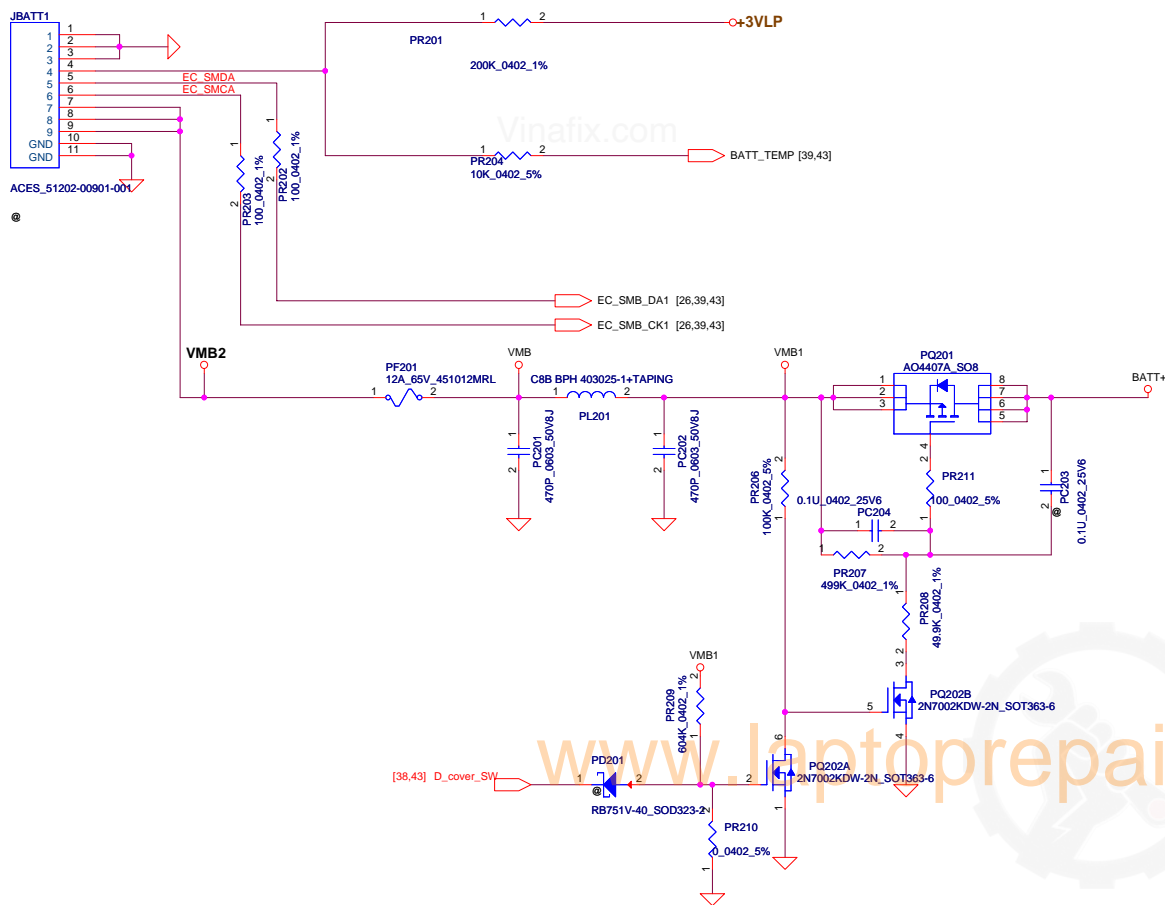
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/01/09	Deciphered Date	2014/01/09	Title	DC Interface
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Date: Tuesday, March 25, 2014				Sheet	40 of 50

ADP_ID

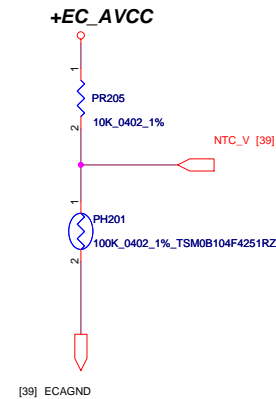
AC Adapter	45W	65W	90W
R(ohm)	118	287	549
ADP_ID(V)	0.449	0.913	1.395
Detection	<=0.663,	<=1.134,	<=1.618
-Voltage(V)	>0.234	>0.693	>1.172



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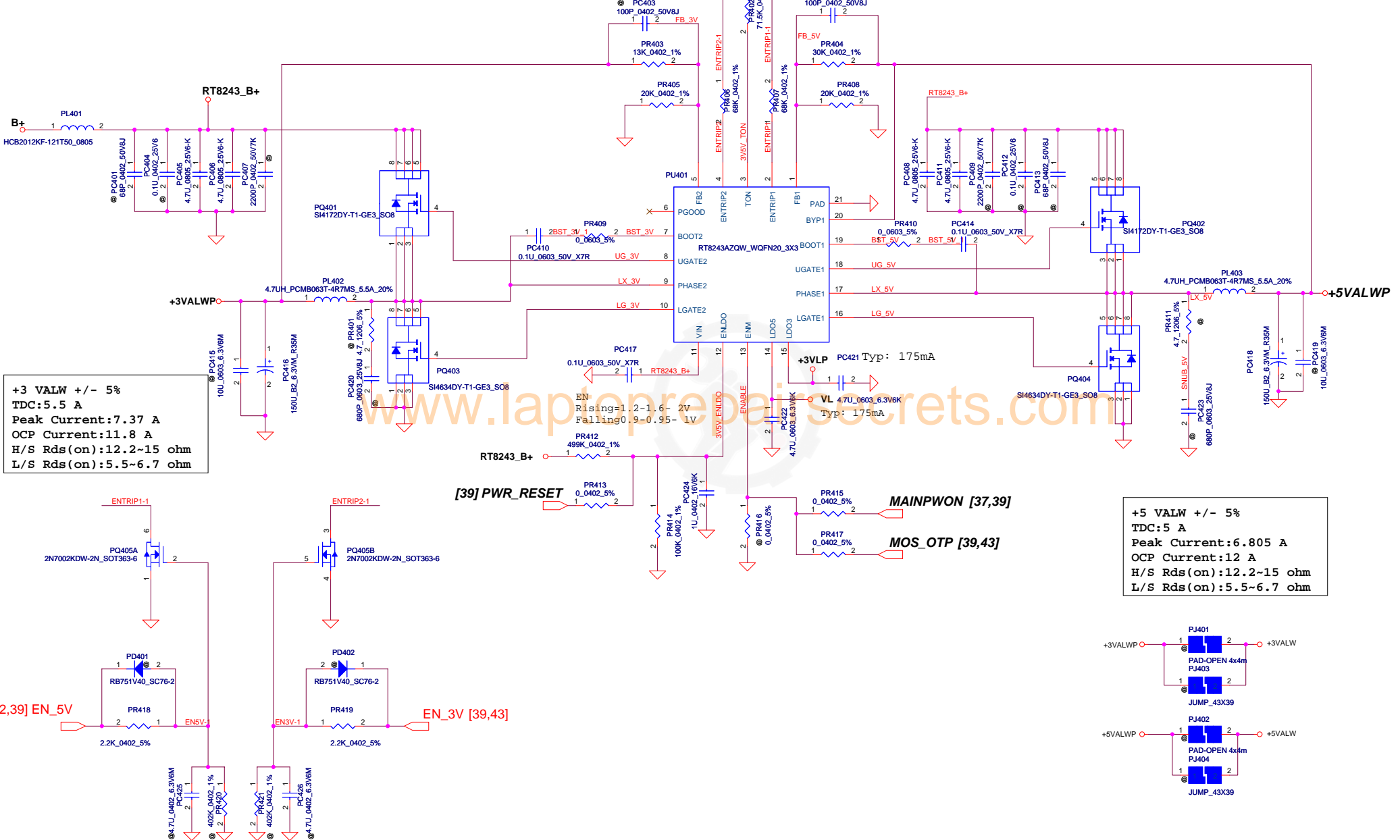
PH201 under CPU botten side :
CPU thermal protection at 93 degree C



PH201:	Temp.	Rman.	Rnor.	Rmin. (Kohm)
	93	7.3419	7.0792	6.8253

TON (1)SMPS1=305KHZ (+5VALWP)
(2)SMPS2=357KHZ(+3VALWP)

Vinafix.com



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Date: Tuesday, March 25, 2014				Sheet 44	of 50

Module model information: RT8812-2Phase

Remark:

- Switching frequency setting: (Ton pin)
 $F_{sw} = (V_{in} - 0.5) / (2 * V_{in} * R_{ton} * 3.2p)$
= 448KHz
- Soft-Start: (SS pin)
SS time (Internal) is 0.7ms (PC18 un-pop)
SS time (External): (PC18 pop)
 $T_{ss} = (C_{ss} * V_{refin}) / I_{ss} + 2.3ms$
= $0.01u * 0.9V / 5uA + 2.3ms = 4.1ms$

4. Current Limit threshold setting
 $R_{ocset} = (I_{valley} * R_{ds(on)} + 40 mV) / 10uA$

$$I_{ripple} = (20 - 1.028) * 1.028 / (448KHz * 0.22u * 20) = 9.89A$$

$$OCP = 72A / 2 = 36A \text{ per phase}$$
$$I_{valley} = 36A - 9.89A / 2 = 31.055A$$

H-side MOS: TPCA8065 L-side MOS: TPCA8057
Rds(on): 11.7mohm @ Vgs=10V 2.0mohm @ Vgs=10V
9.4mohm @ Vgs=4.5V 2.6~3.2mohm @ Vgs=4.5V
Id: 16A @ Ta=25 degC Id: 42A @ Ta=25 degC

5. OpenVReg Configurations: (PSI pin)

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V

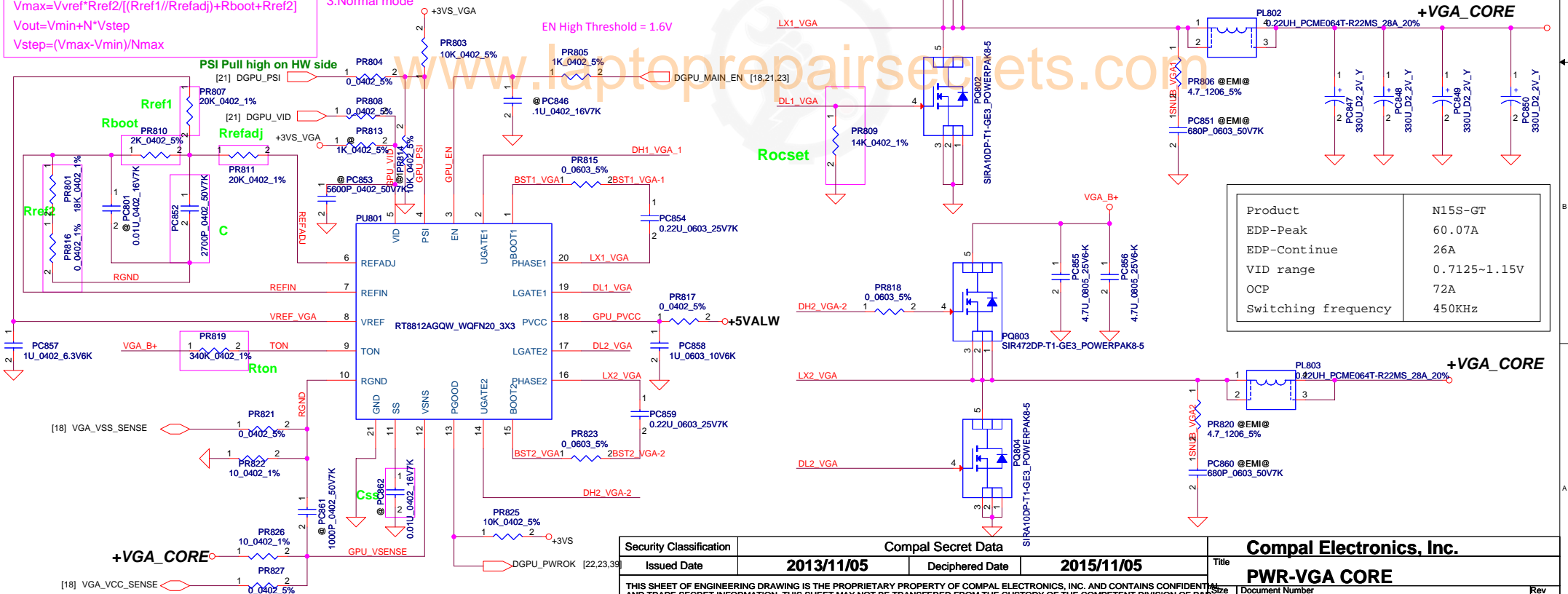
3. PWM-VID Spec and component Values

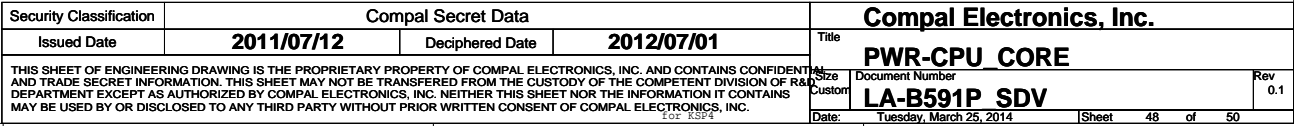
PWM-VID Spec		Config A	Config B	Config C	Config D
Vmin		0.6V	0.6V	0.65V	0.9V
Vmax		1.2V	1.2V	1.15V	1.15V
Vboot		0.875V	0.9V	0.9V	1.028V
Voltage step		6.25mV	6.25mV	25mV	12.5mV
N of Voltage level		96	96	20	20
Rrefadj	PR811	39K	20K	39K	27K
Rref1	PR807	39K	20K	30K	7.5K
Rboot	PR810	1.5K	2K	3K	0
Rref2=PR20+PR21	PR801	30K	18K	24K	6.2K
	PR816	1.5K	0	3K	1.74K
C	PC852	1.5nf	2.7nf	1.8nf	5.6nf

$V_{boot} = V_{ref} * R_{ref2} / (R_{ref1} + R_{ref2} + R_{boot})$
 $R_t = R_{refadj} // (R_{boot} + R_{ref2})$
 $V_{min} = V_{ref} * [R_{ref2} / (R_{ref2} + R_{boot})] * [R_t / (R_{ref1} + R_t)]$
 $V_{max} = V_{ref} * R_{ref2} / [(R_{ref1} // R_{refadj}) + R_{boot} + R_{ref2}]$
 $V_{out} = V_{min} + N * V_{step}$
 $V_{step} = (V_{max} - V_{min}) / N_{max}$

PWM VID and Output voltage control

- Boot mode
- Standby mode (don't support)
- Normal mode



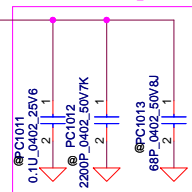
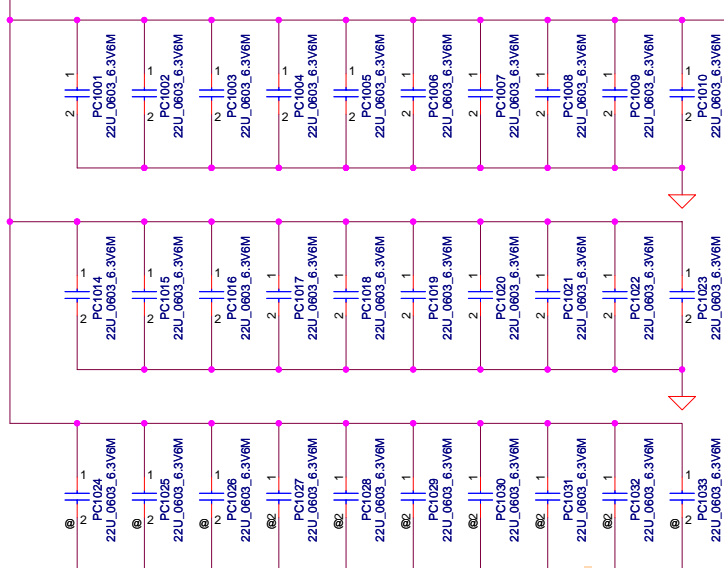


+CPU_CORE

30 X 22u/0603

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RF request



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Date: Tuesday, March 25, 2014				Rev	0.1
Sheet 49 of 50					

Item	Reason for change	PG#	Modify List	Date	Phase
1	Vinafix.com				
2					
3					
4					
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17					

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Date: Tuesday, March 25, 2014				Sheet 50 of 50	